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Low-Power High-Speed ADC Design Techniques in Scaled CMOS Process

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Low-Power High-Speed ADC Design Techniques in Scaled CMOS Process

by

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DISSERTATION

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

DOCTOR OF PHILOSOPHY

THE UNIVERSITY OF TEXAS AT AUSTIN

December 2017

Dedicated to Sinah, Mom, Dad, and Dayeon.

Acknowledgments

First, I sincerely thank my beautiful wife Sinah for always being by my side and instilling positive thinking. Without her, I would not be able to pull through all the encountered obstacles. I thank my parents, my sister, and grandparents for trusting me and praying for me all the time. They were there, when I needed them, and that was all I needed. I honestly cannot thank enough Professor Sun for everything he provided for me. Professor Sun is amazing. He is always inspiring, full of energies, and very supportive. Honestly, compared to all his brilliant students, I am not that bright. Nevertheless, he gave me a chance and allowed me to join his lab, which was a game changer of my life. With all his full-support, I did a state-of-the-art research and I learned more than what I could have imagined. Most importantly, I learned how to analyze and tackle the problems, and how to deliver my ideas to people. And I met Kareem, my mentor. He taught me how to design circuits, set up a test bench, and run simulations. Sometimes, I asked dumb questions but he did not laugh on me but patiently went over the problems with me, again. I would not be able to stand here without his help. And I met all these great people: Arindam, Long, Wenjuan, Yeonam, Xiyuan, Sungjin, Shaolan, Abhishek, Miguel, Linxiao, Chen-kai, and Wenda. They are all brilliant people who are always willing to lend a help when I needed one. I cannot imagine how my life would have changed without any of these people. Last, I would like

to thank Kunhee, Taewoo, Heechai, Jiwon, Kyung Taek, Sejin, and Hyoyoung for making my life a lot more happy. And finally, I sincerely thank you God for always leading me to the right path.

Low-Power High-Speed ADC Design Techniques in Scaled CMOS Process

Publication No. _____

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The University of Texas at Austin, 2017

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The power consumption of a single-channel successive approximation register (SAR) analog-to-digital (ADC) tends to linearly increase with its sampling rate (f_s), when f_s is small. However, when f_s passes a certain point for a given technology node, the ADC power P increases at much higher rate and the normalized power efficiency (P/f_s) starts to degrade rapidly. To enhance the conversion speed of SAR ADC, while maintaining a good power efficiency, this thesis presents speed-enhancing techniques for SAR ADC in nano-scale CMOS technologies. First chapter presents a 2b/cycle hybrid SAR architecture with only 1 differential capacitor-DAC (CDAC). Unlike prior multi-bit/cycle SAR works that make use of only the DAC differential mode (DM) voltage, the proposed architecture exploits both the DM and the common mode (CM). By using two degrees of freedom, 2b/cycle conversion technique can boost the f_s of the ADC without any additional DAC arrays. High-speed ADCs can boost the conversion speed not only by increasing the f_s of a single-channel ADC,

but also by time-interleaving multiple ADC sub-channels running at a lower rate. For an N-channel time-interleaved (TI) SAR ADC operating at f_s, each sub-SAR channel only needs to operate at f_s/N. Therefore, each sub-SAR can operate in the linear power versus speed region, leading to a significant power saving compared to a single-channel ADC running at the same sampling rate. Despite of its power efficiency, TI-ADC suffers from mismatches among sub-ADC channels, including gain, offset, and timing mismatches. Among them, timing skew is one of the most difficult errors to calibrate as it is nontrivial to extract and its induced error depends on both the frequency and the amplitude of the input signal. Second chapter of this thesis presents a TI-SAR with a fast variance-based timing-skew calibration technique. It uses a single-comparator based window detector (WD) to calibrate the timing skew. The WD suppresses variance estimation errors and allow precise variance estimation from a significantly small number of samples. It has low-hardware cost and orders of magnitude faster convergence speed compared to prior variance-based timing-skew calibration technique. The last chapter presents another TI-SAR with mean absolute deviation (MAD) based timing-skew calibration technique. In addition to all the advantages presented with the fast variance-based timing-skew calibration technique, the proposed technique further reduces the digital computation power by 50% by eliminating the squaring operations, which are essential in variance-based calibration technique.

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Chapter 1

2b/cycle Conversion Technique with a Single Differential DAC

A 2b/cycle hybrid successive- approximation-register (SAR) analog-to-digital-converter (ADC) architecture with only 1 differential capacitor-DAC (CDAC) is presented[1]. Unlike prior multi-bit/cycle SAR works that make use of only the DAC differential mode (DM) voltage, the proposed architecture exploits both the DM and the common mode (CM). By using two degrees of freedom, the proposed ADC can generate 3 comparison levels needed for 2b/cycle without requiring extra DAC arrays. Eliminating extra DAC arrays reduces hardware cost, area, and power. The proposed SAR ADC takes advantage of 1b/cycle conversion mode and sufficient redundancy to address problems of multi-bit/cycle conversions, such as unmatched comparator offsets, kick-back noise, and comparator input CM voltage variation. Reconfiguration to 1b/cycle is easily done by disabling the unneeded comparators for 1b/cycle conversion. A 10b prototype ADC is fabricated in 40nm LP CMOS process. It achieves peak 8.5b ENOB at sampling frequency of 300MS/s and consumes

[1]Parts of this chapter are based on: J. Song, X. Tang, and N. Sun, "A 10b 2b/cycle 300MS/s SAR ADC with a single differential DAC in 40nm CMOS," in *IEEE Custom Integrated Circuits Conference* (CICC), 2017, pp. 1–4. The author of this thesis fabricated the prototype chip, performed the measurements, and wrote the published paper.

2.1mW, leading to a FoM of 19.3fJ/conv-step.

1.1 Introduction

SAR ADC is often used for low-speed applications due to its sequential operation, which requires N clock cycles to convert N bit. Recently, various innovative design architectures to enhance the conversion speed of SAR ADCs are studied. Asynchronous clocking architecture boosts the conversion speed by removing any idle conversion time among conversion cycles [1]. Using dedicated comparator for each bit conversion, loop-unrolled architecture increases the conversion speed by removing comparator reset time, and logic and memory delay between comparator and capacitor-DAC (CDAC) [2] - [4]. Multi-bit per cycle conversion technique converts 2b or 3b in a single cycle and enhance the conversion speed [5] -[9]. To generate required reference voltages for multi-bit per cycle architectures, [7] has utilized a resistor-DAC to generate required comparison voltages for 2b/cycle conversions. The resistor-ladder DAC, however, requires large number of switches and routings, and static current flows, which significantly increases power. Reference CDACs [6], resistor and capacitor mixed-DAC with sub-ranging techniques [8], custom-designed compact CDAC [5], and CDAC interpolation [9] are studied. They replaced the resistor-DAC and reduced static power. These techniques, however, still require multiple differential capacitor-DACs, resulting in substantially increased hardware complexity, area, and power. This chapter presents a 2b/cycle hybrid SAR architecture that uses only 1 differential capacitor-DAC to enable

2b/cycle conversions. Moreover, unlike prior works that make use of only the DAC differential mode (DM) voltage, this new architecture exploits both the DM as well as the common mode (CM). By using two degrees of freedom, it generates 3 comparison levels needed for 2b/cycle without requiring extra DAC arrays. The proposed ADC thus reduces power and area, occupied by extra DACs and its control logic blocks. The proposed ADC is a hybrid SAR that takes an advantage of both 2b/cycle and 1b/cycle conversion modes. 2b/cycle conversion technique boosts the conversion speed by 2x and 1b/cycle conversion mode addresses problems of multi-bit/cycle conversions, including comparator offsets, noise, and CM voltage variations [6]. Moreover, sufficient redundancy is embedded to adequately absorb errors from such problems. Reconfiguration from 2b/cycle to 1b/cycle mode is simply done by disabling comparators used in 2b/cycle conversion mode, similar to a hardware retirement technique of [6]. A prototype is implemented in 40nm LP CMOS. It achieves a peak 8.5b ENOB at 300MS/s sampling rate and consumes only 2.1mW, leading to a FoM of 19.3fJ/conv-step.

1.2 Proposed ADC Architecture

Fig. 1.1 illustrates an example 5b conversion of analog input "7" with the proposed architecture. During the sampling phase (step 1), differential inputs, V_{inp} and V_{inm}, are sampled onto DAC top plates. After sampling (step 2), the DAC CM voltage is raised by $\frac{1}{2}V_{ref}$ (V_{ref} is the reference, given by V_{refp}-V_{refm}). First comparator (CMP1) compares $V_{inp} + \frac{1}{2}V_{ref}$ with the

input CM voltage V_{cmi} (indicated as 0 for simplicity), where V_{cmi} is given by $(V_{refp} + V_{refm})/2$. Second comparator (CMP2) compares $V_{inp}+\frac{1}{2}V_{ref}$ with $V_{inm}+\frac{1}{2}V_{ref}$, and the third comparator (CMP3) compares $V_{inm}+\frac{1}{2}V_{ref}$ with V_{cmi}. As shown in the Fig. 1.1, these comparisons are equivalent to comparing the differential input $\Delta V \equiv V_{inp} - V_{inm}$ to $\pm V_{ref}$ and 0, and thus, achieve 2b. After the DAC DM voltage is updated, the same process repeats (step 3). The DAC CM voltage is now raised by $\frac{1}{8}V_{ref}$, and 3 comparators compare the residual to $\pm\frac{1}{4}V_{ref}$ and 0 to obtain another 2b. As shown in step 2 and 3, the proposed SAR makes use of both DAC CM and DM voltages to convert 2b per cycle without any extra DAC arrays. This is the key idea that differentiate this work from prior works, which require extra DAC arrays for 2b/cycle operations. Finally, in step 4, CMP1 and CMP3 are disabled, and the SAR easily reconfigures to 1b/cycle conversion mode.

Because 2b/cycle conversion mode requires 3 comparators, its accuracy suffers from unmatched comparator offsets, kickback noise, and comparator input CM voltage variation. The proposed ADC makes use of redundancy and 1b/cycle conversion mode to address such problems. Embedded redundancy by reducing the MSB capacitor size as well as a 1 redundant bit during the transition from 2b/cycle to 1b/cycle sufficiently absorb errors from above problems. Moreover, 1b/cycle conversion mode is free from CM voltage variations and it can easily address these problems [6]. Although 1b/cycle is slower than 2b/cycle, it is needed only for few LSBs, and thus, the ADC overall speed penalty is low, leading to a good balance between speed and accuracy.

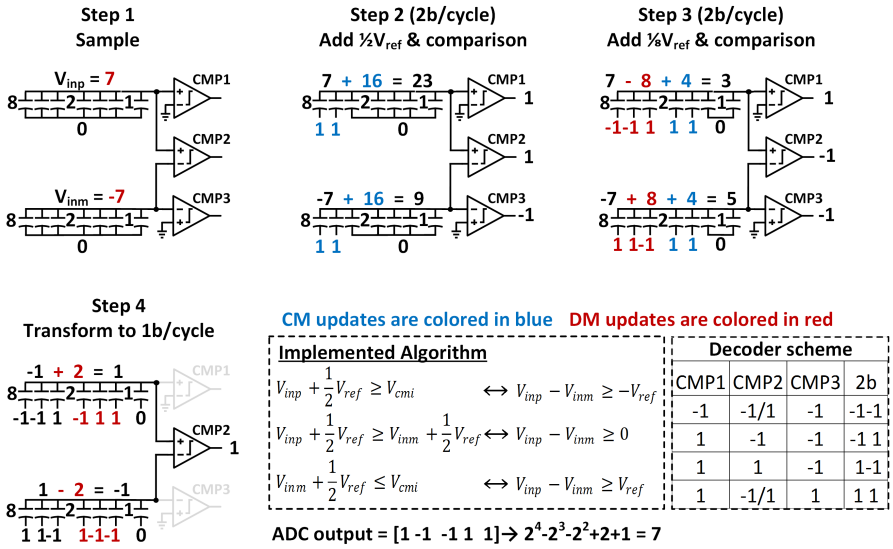

Figure 1.1: The Proposed ADC conversion example of analog input "7".

The proposed architecture performs 3 2b/cycle conversions and 5 1b/cycle conversions. Fig. 1.2 depicts the block diagram of the proposed SAR architecture. The proposed ADC consists of a single differential DAC, 3 bootstrap switches, 3 comparators, a control logic, and a clock generator. Bootstrap switches sample V_{inp} and V_{inm} onto the CDAC and V_{cmi} on C_{mid}. The reason to sample V_{cmi} is to tolerate V_{cmi} variation and ensure the same CM voltage at CMP1 and CMP3 (V_{cmi} is assumed to be available here; if not, it can be easily obtained by using 2 C_{mid} capacitors to sample V_{inp} and V_{inm}, and then merging them to obtain V_{cmi}). The capacitance-size of the C_{mid} is equivalent to a sum of capacitances of a single DAC array. It makes comparator input nodes equally encounter kickback noise of the comparators. The clock generator drives CMP1 and CMP3 for only 3 cycles and CMP2 for 8 conversion cycles so that CMP1 and CMP3 do not activate when the proposed ADC is

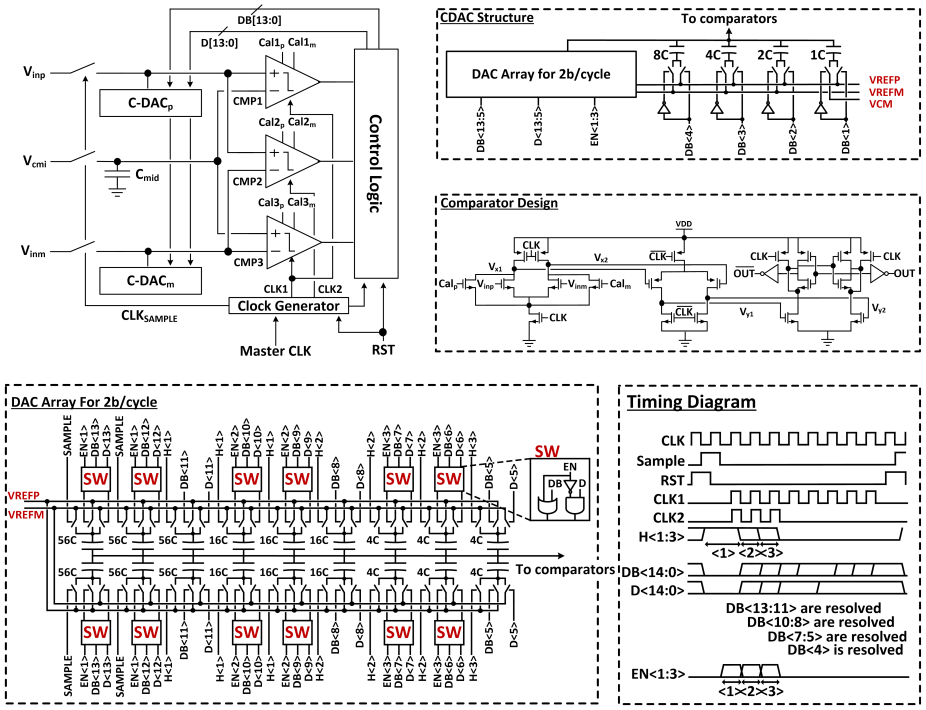

Figure 1.2: The proposed ADC architecture and the design of CDAC and the proposed 3-stage comparator.

in the 1b/cycle conversion mode.

1.3 Circuit Implementation

In Fig. 1.2, the design of the 3-stage dynamic comparator and the CDAC architecture are illustrated. The proposed comparator comprises 3 stages. When the clock is high, the input transistors begin to discharge V_{x1} and V_{x2} nodes that drive the PMOS input pairs of the second stage. When these nodes become sufficiently low, the nodes V_{y1} and V_{y2} get charged toward VDD. When these nodes are suitably charged, the third stage starts the regeneration

phase. Due to positive feedback from the cross coupled inverters and pre-amplification gain from the first two stages, outputs regenerate quickly. Large pre-amplification gain from the first two dynamic integration stages sufficiently reduces the regeneration time to help meeting the timing specification of the proposed architecture. Comparator offset is foreground calibrated by adjusting Cal_p and Cal_m. Since DAC redundancy is provided after 2b/cycle conversions and can tolerate as large as 10mV offset mismatch among 3 comparators, the proposed ADC does not need precise comparator mismatch calibration. Only coarse calibration is enough to achieve the targeted performance specifications. Fig. 1.2 also illustrates a block diagram of the CDAC. The total CDAC size is 935C and the unit capacitor is 0.5fF. The MSB capacitor size is reduced from 128C to 112C to tolerate CM voltage variations and incomplete settling errors. Similarly, a redundant 8C capacitor is used to sufficiently absorb errors from 2b/cycle operations. The DAC array associated with the 2b/cycle operation and the timing diagram of its control signals are shown more in detail in Fig. 1.2. Three sets of 3 capacitors, {112C, 32C, 8C}, are employed for 6b conversions. During each 2b/cycle, 3 capacitors of each set are directly driven by the 3 comparator outputs without the need for any encoding logic. All capacitors in 2b/cycle DAC are split to two (e.g., 112C→ {56C, 56C}) for faster reset to V_{cm} during the sampling phase. These capacitor arrays are controlled by 4 signals, including D<13:5>, DB<13:5>, EN<1:3>, and hold signal H<1:3>. During the sampling phase (see Fig. 1.1), all signals are reset to 0 except H<1:3>, which are raised to set the first half of the split

DAC to V_{refp} and the second half to V_{refm}, and thus resetting the DAC to V_{cm}. As mentioned earlier, the DAC CM voltage needs to be raised during 2b/cycle conversions. This is done without using extra DAC arrays. Instead, EN<1:3> signals switch the bottom plates of appropriate capacitors from V_{refm} to V_{refp}. As a result, $\frac{1}{2}V_{ref}$, $\frac{1}{8}V_{ref}$, and $\frac{1}{32}V_{ref}$ are added to the DAC CM voltage. D<13:5> and DB<13:5> reconfigure the DM of DAC according to the comparison results. D<13:11>, D<10:8>, and D<7:5> correspond to the 3 comparator outputs during each of the 3 2b/cycle comparisons. When 2b/cycle conversions finish and transit to 1b/cycle conversion mode, DAC CM voltage is now fixed and only DM voltages change. As shown in the CDAC structure of Fig. 2, DB<4:1> reconfigures the DM of the DAC arrays {8C, 4C, 2C, 1C} associated with 1b/cycle conversions. DB<0> is the last comparison result and it does not drive the DAC. DB<4:0> are the comparison results of CMP2, which is only active during the 1b/cycle conversions. Unlike the capacitors in 2b/cycle conversions that must reset to V_{cm} during the sampling phase, {8C, 4C, 2C, 1C} capacitors do not need to reset to V_{cm}. Thus, {8C, 4C, 2C} capacitors resets to ground and only the last 1C resets to V_{cm}. 1C is reset to V_{cm} because it applies bidirectional single-side switching technique [10]. Last, the SAR control logic and clock generator are implemented using dynamic logic to save power and shorten delay.

1.4 Measurement Results

The prototype is fabricated in 40nm LP CMOS. It occupies an active area of $95 \times 90\mu m^2$ as shown in Fig. 1.3. The ADC output is decimated by 8 to simplify the measurement process. Operating at 300MS/s under 1.2V supply, the prototype consumes 2.1mW (analog: 0.3mW, digital: 1.4mW, and reference: 0.4mW). Fig. 1.4 shows measured ADC output spectra. With 1MHz input, the measured SNDR and SFDR are 53dB and 69dB, respectively. With 140MHz input, the SNDR and SFDR are 47dB and 63dB, respectively. Fig. 1.5 shows measured SNDR and SFDR versus the input frequency, the input amplitude, and the sampling frequency. SNDR stays above 50dB with input frequency between 1MHz and 90MHz and above 47dB with input frequency up to Nyquist. SNDR is observed to be flat and above 53dB with the sampling speed from 100MS/s to 300MS/s. The measured INL and DNL are +1.3/-1.1 LSB and +1.3/-1.0 LSB, respectively. Table I summarizes the performance and compares it to recent multi-bit/cycle works. As shown in Table I, the performance of the proposed ADC is comparable to other state-of-the-arts.

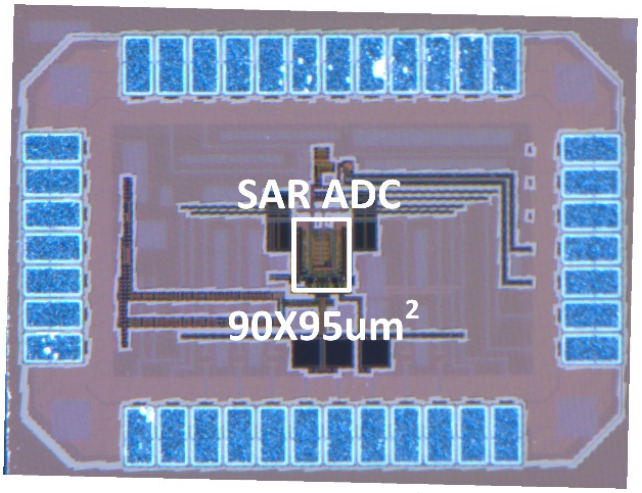

Figure 1.3: Die photo.

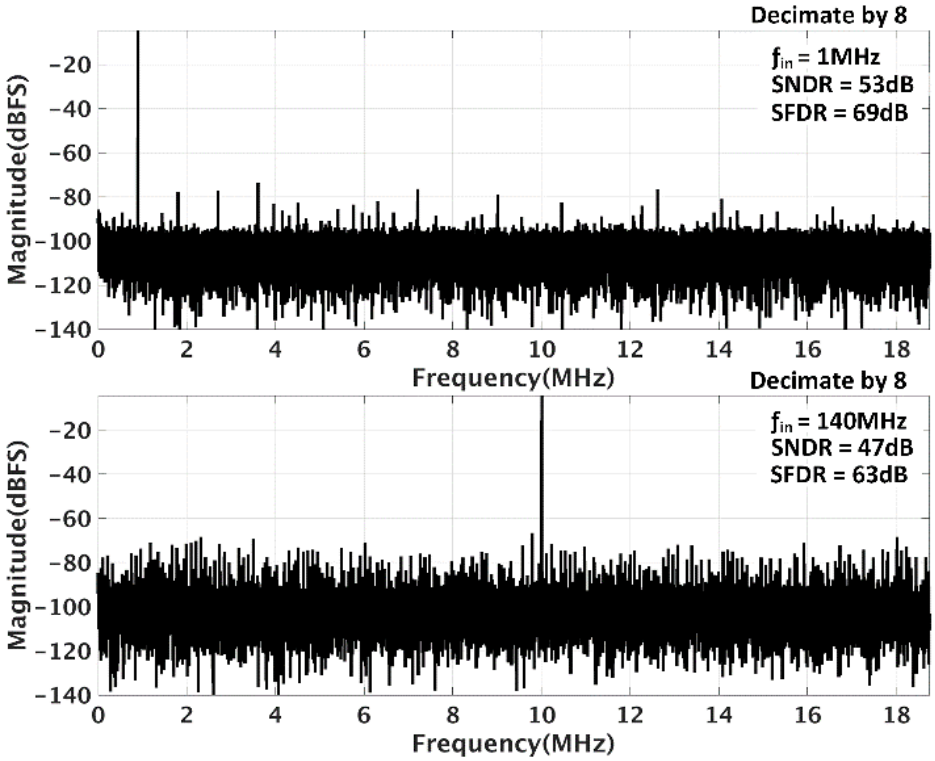

Figure 1.4: Measured FFT spectrum with 1MHz and near-Nyquist input (decimated by 8).

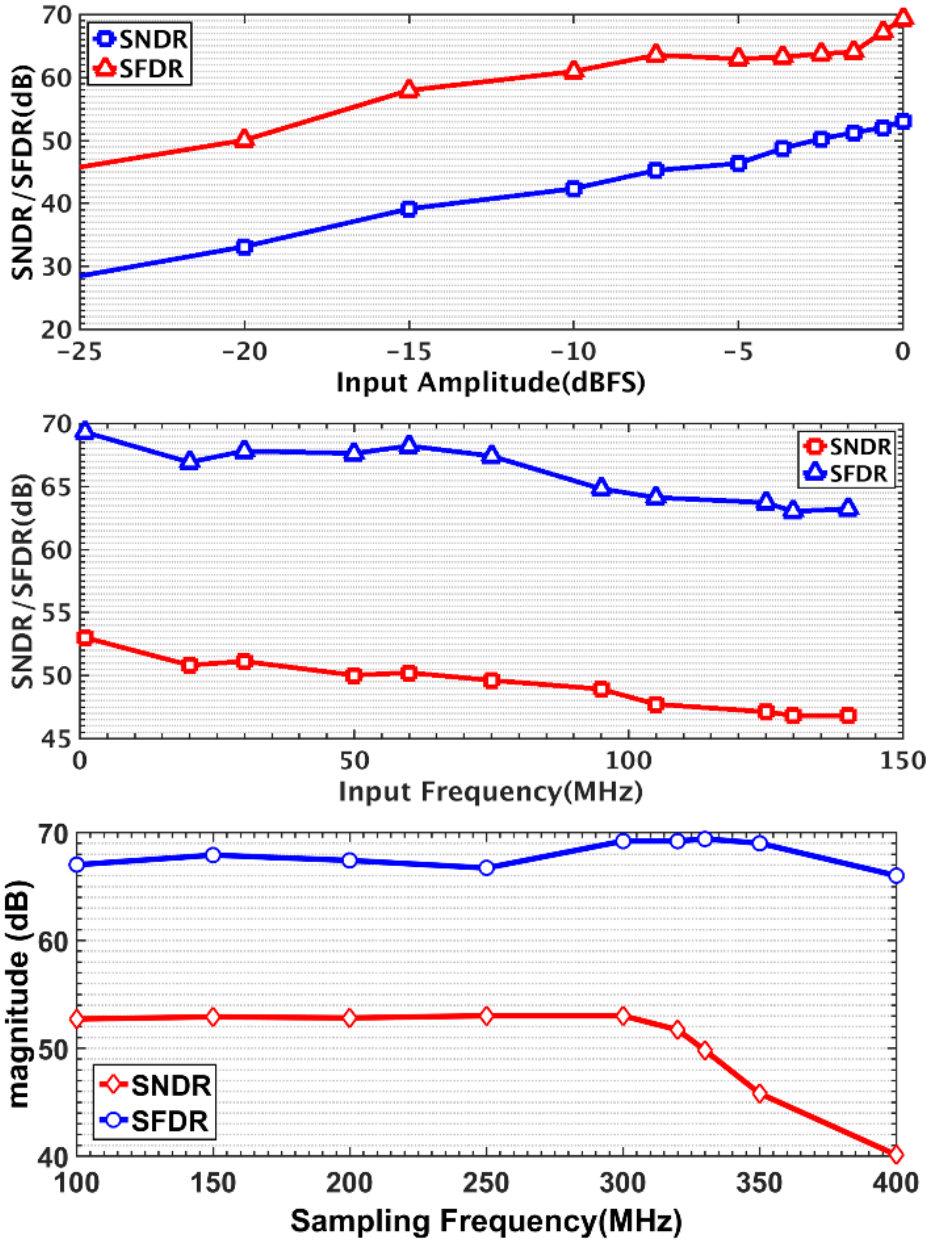

Figure 1.5: Measured SNDR and SFDR versus input frequency, input amplitude, and sampling frequency.

Parameters	[5]	[6]	[7]	[8]	**This work**
Architecture	2.6b SAR,TI	2b SAR	2b SAR	2b SAR, TI	**2b SAR**
Technology [nm]	45	65	28	65	**40**
♯ of Differential DAC	3	2	2	2	**1**
Fs [MS/s]	⋆425	250	750	⋆500	**300**
Resolution [bit]	10	8	8	8	**10**
Power [mW]	⋆⋆3.9	1.8	4.5	⋆⋆1.9	**2.1**
SNDR [dB]	55.3	46.7	45.2	45.8	**53.0**
SNDR @Nyquist [dB]	51.2	43	43.3	42.8	**47.0**
Active Area [mm^2]	⋆⋆0.014	0.024	0.004	⋆⋆0.007	**0.008**
Peak FoM [fJ/conv]	19	42	41	24	**19**

⋆Sampling frequency of a single channel

⋆⋆Divided by ♯ of interleaved channels for comparison

Table 1.1: Performance summary and comparison

Chapter 2

Variance-based Fast Timing-Skew Calibration

This chapter presents a time-interleaved (TI) SAR analog-to-digital converter (ADC) with a fast variance-based timing-skew calibration technique[1]. It uses a single-comparator based window detector (WD) to calibrate the timing skew. The WD can suppress variance estimation errors and allow precise variance estimation from a significantly small number of samples. It has low-hardware cost and orders of magnitude faster convergence speed compared to prior variance-based timing-skew calibration technique. The proposed technique brings collateral benefit of offset mismatch calibration. After timing-skew calibration, a prototype 10-b 800-MS/s ADC in 40-nm CMOS achieves the Nyquist-rate SNDR of 48 dB and consumes 4.9 mW, leading to the Walden FoM of 29.8-fJ/conversion step. This chapter is organized as follows. Section 2.2 introduces the proposed timing-skew calibration technique. Section 2.3 presents the convergence time analysis and the choice of the window width. Section 2.4 discusses the practical design issues and the limitations of the

[1]Parts of this chapter are based on: J. Song, K. Ragab, X. Tang, and N. Sun, "A 10-b 800-MS/s Time-Interleaved SAR ADC With Fast Variance-Based Timing-Skew Calibration," *IEEE Journal of Solid-State Circuits,* vol. 52, no. 10, pp. 2563–2575, Oct. 2017. The author of this thesis fabricated the prototype chip, performed the measurements, and wrote the published paper.

proposed technique. Measurement results are shown in Section 2.5.

2.1 Introduction

The power consumption of a single-channel analog-to-digital converter (ADC) tends to linearly increase with its sampling rate (f_s), when f_s is small. However, when f_s passes a certain point for a given technology node, the ADC power P increases at much higher rate and the normalized power efficiency (P/f_s) starts to degrade rapidly [11]. Thus, state-of-the-art high-speed ADCs boost the conversion rate not only by increasing the speed of a single-channel ADC, but also by time-interleaving multiple ADC channels running at a lower rate [11]–[23]. For an N-channel time-interleaved (TI) ADC operating at f_s, each sub-ADC channel only needs to operate at f_s/N. Therefore, each sub-ADC can operate in the linear power versus speed region, leading to a significant power saving compared to a single-channel ADC running at the same sampling rate. Despite of its power efficiency, TI-ADC suffers from mismatches among sub-ADC channels, including gain, offset, and timing mismatches. Among them, timing skew is one of the most difficult errors to calibrate as it is nontrivial to extract and its induced error depends on both the frequency and the amplitude of the input signal. It is known to be a performance bottleneck for TI-ADCs. To reduce timing mismatches, various timing-skew calibration techniques have been developed. In [15] and [16], a foreground timing-skew calibration technique without an extra ADC channel is presented. A signal generator applies a test signal to the TI-ADC, and the

relative timing information of sub-channel ADCs is extracted with a Fourier analysis. One limitation of this technique, however, is that it cannot track process, voltage, and temperature (PVT) variations because the system must interrupt the normal ADC operations until the calibration is complete. In [17]–[19], background timing-skew calibration with a dedicated reference channel is reported to address the limitation of the foreground calibration techniques. In [17], a full-blown reference ADC is employed for the calibration. In [18], two reference ADCs are utilized. One is used to estimate the input derivative and the other one functions as a timing-skew free reference. Despite their effectiveness, additional full-blown ADC replicas can substantially increase power and hardware overhead, especially when the interleaved number of channels (N) is small. Also, Chen and Pileggi [17] and Stepanovic and Nikolic [18] set a lower limit on the alignment (beat) period of the reference and each sub-ADC channels to $N(N+1)$ clock cycles, which reduce the calibration speed. Moreover, the alternatingly operated reference can introduce spurs by periodically changing the overall TI ADC input impedance [24]. In [19], the reference channel is simplified to a single comparator to minimize the power and hardware overhead. Nevertheless, the convergence speed of its algorithm is slow for random inputs when it runs in background due to large random variations in the autocorrelation estimation process. The works of [11], [20], and [21] present techniques to calibrate the timing skew in background without an additional reference. Without a separate reference, the ADC input impedance remains constant and no spurs arise from impedance variations. Nonetheless, Wei et

al. [11] and Lin et al. [21] have a tight requirement on the shape of the ADC input autocorrelation function, and Dortz et al. [20] have a restriction on input characteristics that input signals must not be close to or above Nyquist rate. In [22] and [23], flash-assisted TI (FATI) SAR ADCs are proposed to address limitations such as tight input restriction and input-impedance variation by having a low-resolution flash ADC running at the ADC full rate. Thanks to the flash, each SAR channel can run faster. However, a flash ADC is power consuming. Lee et al. [22] remove the timing skew by reducing the variance of each SAR channel output. It is robust against the comparator offset and noise, but its convergence speed is slow when it operates in background with unknown inputs that can cause large fluctuations in the variance estimation.

This chapter presents a novel variance-based timing-skew calibration technique for TI ADC. It exploits the relationship between the comparator input and its decision time to identify ADC inputs that are close to the comparator threshold. By using only these samples, the variance computation has much smaller estimation errors. Thus, the proposed technique substantially reduces the number of samples needed to obtain an accurate variance estimation and significantly boosts the convergence speed. Simulation results show that when running in background with random inputs, the convergence speed of the proposed technique is orders of magnitude faster than that of the prior variance-based timing-skew calibration technique of [22]. Furthermore, the proposed technique obviates the need for a flash ADC; instead, it only requires a single-comparator-based window detector (WD), which reduces hardware overhead

and power. To verify the proposed technique, a prototype 10-b 800-MS/s ADC is built in 40-nm CMOS. It consumes 4.9 mW and achieves a post-calibration Nyquist-rate signal-to-noise-and-distortion ratio (SNDR) of 48 dB, leading to a Walden Figure-of-Merit (FoM) of 29.8-fJ/conversion step.

2.2 Time-Interleaved ADC with the Proposed Variance-based Timing-skew Calibration

2.2.1 Circuit Implementation

Fig. 2.1 shows the architecture of a four-way TI SAR ADC with the proposed timing-skew calibration technique. It consists of four SAR ADCs, a WD-based reference channel, an output MUX, a multi-phase clock generator, variable delay lines (VDLs), and a variance estimator block. Each of the four sub-ADCs samples the input signal V_{in} at the falling edge of its sampling clock ($\phi_1 \sim \phi_4$). The SAR ADC asynchronously resolves 11-b with 1-b redundancy [25], [26]. After the timing-skew estimation, the variance estimator controls the digitally controlled VDL to closely align the falling edges of $\phi_1 \sim \phi_4$ with those of the WD ϕ_{ref}.

Fig. 2.2 illustrates the block diagram of the WD. It consists of a replica sampling network, a dynamic latch comparator, a current-starved inverter chain, and a flag D flip-flop (DFF). The WD operates at the full ADC rate (f_s) and thus eliminates the potential spurs from input impedance variations.

The variance estimator utilizes the WD to check whether a sampled ADC input V_{in} is within a fixed window, i.e., $|V_{in}| < W$, where W is the window

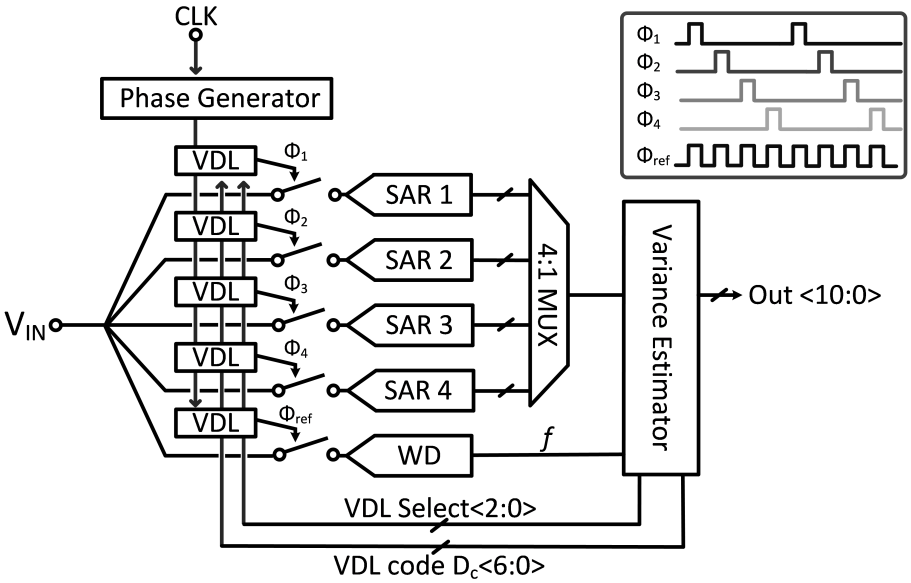

Figure 2.1: Block diagram of a 4-way time-interleaved SAR ADC with the proposed variance-based timing-skew calibration technique.

width. When ϕ_{ref} is high, bootstrap switch samples V_{in} and the comparator is reset. As soon as ϕ_{ref} goes low, the comparator starts regeneration and the clock signal goes into the current-starved inverter chain. The window flag f is raised when the clock signal (delay) arrives at the DFF before the XOR output (XOR) goes high. The inverter chain is configured as $\tau_{delay} = \tau_{comp} + \tau_{XOR}$, where τ_{XOR} is the XOR delay and τ_{comp} is the comparator delay when $|V_{in}| = W$. If $|V_{in}| < W$, the regeneration time of the comparator is longer than that of τ_{comp} and hence raises the flag ($f = 1$). When the flag is high, the variance estimator collects the corresponding ADC output. On the other hand, if $|V_{in}| > W$, the flag f is not raised ($f = 0$). W can be tuned by adjusting τ_{delay} via controlling the bias current (I_B) into the current-

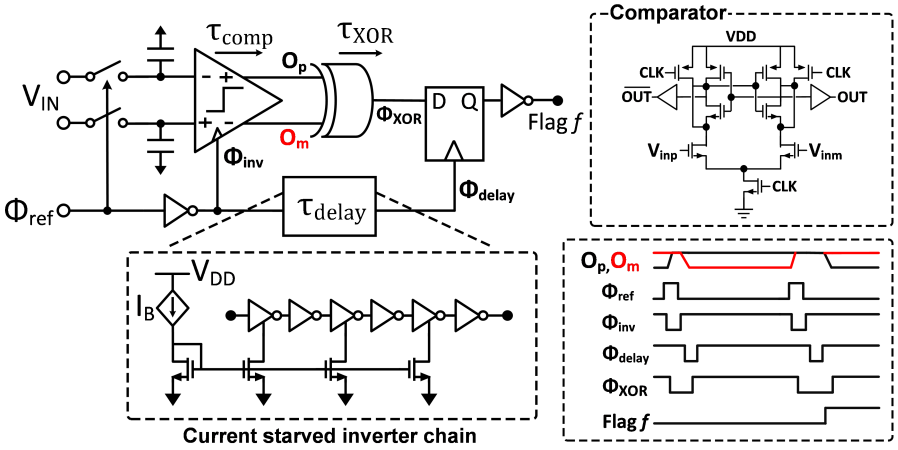

Figure 2.2: Block diagram of the comparator based window detector.

starved inverter chain of the WD. Increasing I_B reduces τ_{delay} as well as W. By contrast, reducing I_B increases τ_{delay} and W.

Fig. 2.3 shows the schematic of the 10-b single-channel ADC. It uses 1/8 of the conversion period for sampling and the rest for 11-b conversions. Totally, 11 comparators are used for each of 11-b conversion. First stage consists of four conversions, and the second stage consists of seven conversions. The unit capacitor C is 2 fF, and the total digital-to-analog converter (DAC) capacitance is 272C, including 16C of redundancy. A modified bidirectional single-side switching scheme of [26] is used to reduce the number of unit capacitors by 4 times compared to that of the conventional SAR switching technique.

The conversion rate of 200 MS/s is achieved by using the loop-unrolled architecture, which greatly reduces the critical path delay [27]–[29]. Offset mismatches of 11 comparators are addressed by using stage segmentation, adding a redundancy bit, and sharing a single-dynamic pre-amplifier [29]. The

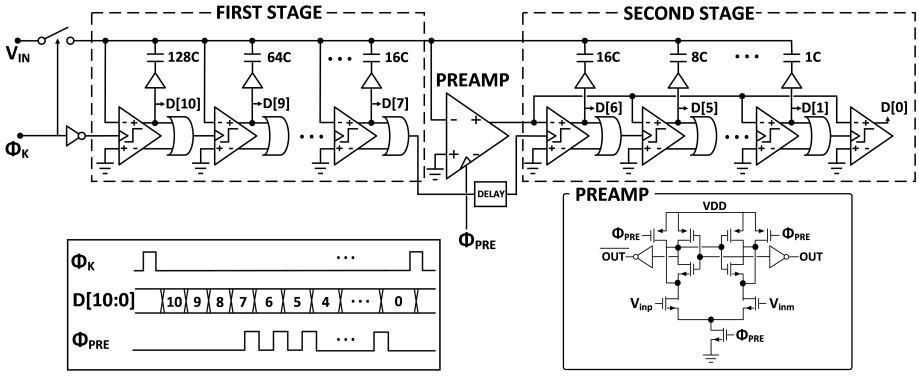

Figure 2.3: Block diagram of the single-channel SAR ADC.

preamplifier is a dynamic latch-based amplifier, driven by the clock ϕ_{PRE}, which is active only in the second stage. The preamplifier amplifies the residual voltages before the comparison so that the residual voltages are not affected by the comparator offset mismatches in the second stage.

Fig. 2.4 shows the block diagram of the multi-phase clock generator. The low-voltage differential-signaling (LVDS) receiver converts $400\text{m}V_{pk-pk,diff}$, off-chip input to a single-ended clock ϕ_0 [30]. The transmission gates are controlled by the outputs ($S_1 \sim S_4$) of 4 DFFs arranged in a ring. One DFF is initialized to 1, and all DFFs are triggered by the falling edge of ϕ_0. This generates four 25%-duty-cycle signals that are 90° apart. Triggering the DFFs with the falling edge of ϕ_0 allows $S_1 \sim S_4$ to not get affected by clk-to-q delay of the DFFs. These pulses control the transmission gates and sequentially pass ϕ_0 every 4 clock cycles. Given that ϕ_0 is 50% duty cycle, each sub-ADC sampling clock has a duty cycle of 1/8. The advantage of this scheme is low jitter as ϕ_0 only passes through the transmission gate, one buffer, and VDLs

to produce $\phi_1 \sim \phi_4$ [31]. Jitters in control pulses ($S_1 \sim S_4$), generated by DFFs, do not affect the critical sampling edges of $\phi_1 \sim \phi_4$.

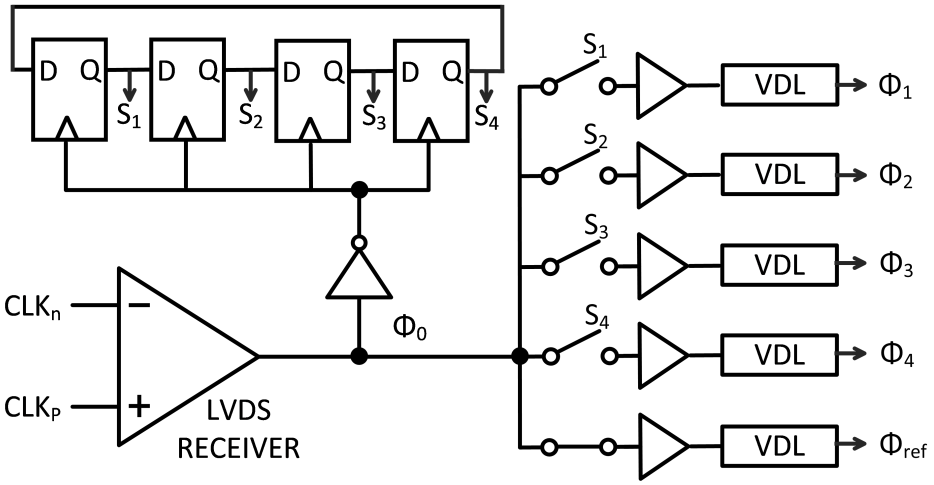

Figure 2.4: Block diagram of the multi-phase clock generator.

Fig. 2.5 shows the block diagram of the VDL. It has 5-bit binary-weighted control code for a fine delay tuning of 300fs per step and 2-bit coarse control code with 2ps per step.

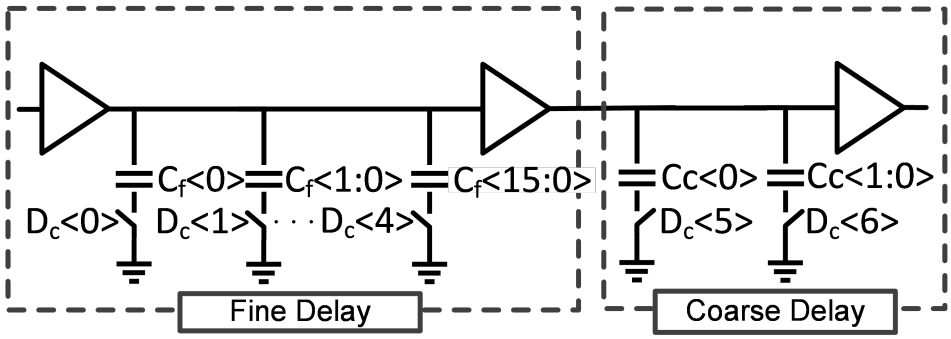

Figure 2.5: Block diagram of the variable delay line for timing-skew calibration.

2.2.2 Basic Idea of the Proposed Timing-skew Calibration Technique

The variance estimator collects all ADC outputs with $f = 1$ and sorts them into 4 sets depending on which channel they come from. The estimator then computes the sample variance for each of the 4 sets. When timing skew between a single-channel ADC and the window detector exists, the collected ADC outputs are scattered to side-corners, which lead to a large variance ($\approx 315LSB^2$), as shown in Fig. 2.6 for a single-tone sinusoidal input.

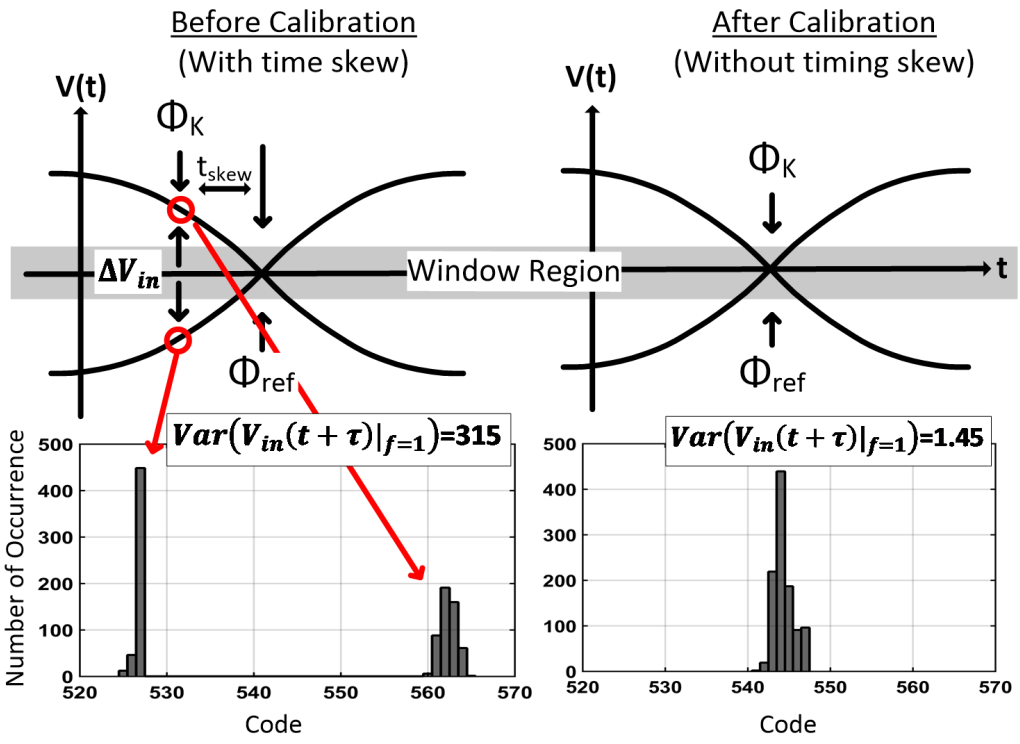

Figure 2.6: Basic idea of the proposed variance-based timing-skew calibration.

By contrast, when the timing-skew between the ADC channel and the

window detector is minimized, the collected ADC outputs are distributed in the center among few codes, which indicates that the variance is at minimum ($\approx 1.45LSB^2$). Thus, the variance is an indicator of the timing skew, which can be reduced by monitoring the sample variance and minimizing it through the VDL delay adjustment.

In addition to timing skew-calibration, the proposed calibration technique collaterally brings the benefit of offset mismatch calibration. When all ADC outputs with $f = 1$ are sorted into 4 sets, offset mismatch is determined by calculating the mean value of each of 4 sets. The offset mismatch can be digitally canceled by subtraction from each channel outputs.

2.2.3 Mathematical Explanation of the Proposed Timing-Skew Calibration Technique

The variance of a single-channel ADC's outputs with $f = 1$, denoted as $\sigma_v^2(\tau)$, can be derived as:

$$\begin{aligned} \sigma_v^2(\tau) &\equiv Var(V_{in}(t+\tau)|_{f=1}) \\ &\cong Var(V_{in}(t+\tau \cdot \frac{dV_{in}}{dt})|_{f=1} = \sigma_v^2(0) + \tau^2 \cdot \sigma_{dv}^2 \end{aligned} \tag{2.1}$$

where τ is the timing skew between the single ADC channel and the window detector, and σ_{dv} represents the standard deviation of $\frac{dV_{in}}{dt}$ conditioning on $f = 1$. In deriving (2.1), $V_{in}(t)$ and $\frac{dV_{in}}{dt}$ are treated as uncorrelated random variables due to their inherent orthogonality. It is clear from (2.1) that $\sigma_v^2(\tau)$ grows quadratically with τ at a rate proportional to σ_{dv} (i.e., input am-

plitude and frequency). To verify the validity of (2.1), behavioral simulations are performed for a 10-bit 800MS/s 4-way TI ADC for single-tone sinusoidal inputs (amplitude at 0.8V and frequencies at 99MHz, 190MHz, 390MHz), two-tone sinusoidal inputs (amplitude at 0.4V each and two frequencies of 290MHz and 390MHz) and a Gaussian random input with a standard deviation of 0.3V and a bandwidth of $[0, 200\text{MHz}]$. Thermal noise is not considered for simplicity. All the performed simulation results include quantization error unless it is noticed. The results are plotted in Fig. 2.7 and match well with (2.1).

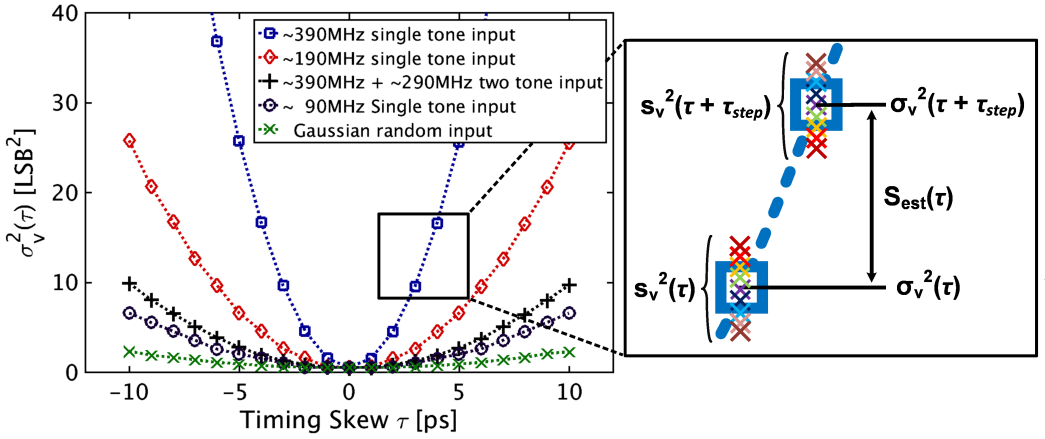

Figure 2.7: Behavioral simulation illustrating the relationship between $\sigma_v^2(\tau)$ and τ.

Fig. 2.7 clearly shows the quadratic relationship. As the input frequency increases, $\sigma_v^2(\tau)$ grows more rapidly. For all cases, $\sigma_v^2(\tau)$ is however minimized at $\tau = 0$. Therefore, by estimating and minimizing $\sigma_v^2(\tau)$, the timing skew can be corrected, which is the basis of the proposed calibration technique.

2.3 Convergence Time Analysis and Choice of the Window Width

Convergence time is an important factor for any timing-skew calibration technique. It must be short enough to keep track of temperature and voltage variations due to their strong influences on the timing skew. For the proposed technique, its convergence time is limited by the number of ADC outputs, M, that is needed in order to ensure an accurate estimation of $\sigma_v^2(\tau)$. Note that $\sigma_v^2(\tau)$ in (2.1) is the expected value of the variance. In practice, $\sigma_v^2(\tau)$ needs to be estimated by calculating the sample variance of real ADC outputs with $f = 1$, which is denoted as $s_v^2(\tau)$ and is given by:

$$\frac{\sum_{m=1}^{M}(V_{in}[m] - V_{avg})^2 f[m]}{\sum_{m=1}^{M} f[m]} \tag{2.2}$$

where V_{avg} represents the sample average, and $f[m]$ is defined as 1 for $|V_{in}[m]| < W$ and 0 otherwise. The effects of the ADC thermal noise and quantization error are ignored in (2.2). They are considered in Section IV. Although $s_v^2(\tau)$ converges to $\sigma_v^2(\tau)$ when M goes to infinity, it is not equal to $\sigma_v^2(\tau)$ for any finite M due to the random nature of the input. To ensure the measured $s_v^2(\tau)$ is close to $\sigma_v^2(\tau)$, M must be sufficiently large, which limits the convergence speed.

For the proposed technique, the key parameter that determines M is the window width, W. At first glance, a larger W is preferred because a larger portion of ADC input samples falls into the window, and hence more

$f = 1$ samples are averaged to estimate more precise variance. However, a larger W substantially increases fluctuations in the variance estimation $s_v^2(\tau)$. Fig. 2.8 shows behavioral simulation results for 4 different W of 6, 12, 24, and 48 LSBs with the same Gaussian random input used in Fig. 2.7. For every W, a total of 100 sample variances $s_v^2(\tau)$ are collected, each of which is computed with $M = 10^5$. Fig. 2.8 clearly shows that the fluctuation in $s_v^2(\tau)$ significantly increases with W. The variation in $s_v^2(\tau)$, denoted as σ_s^2, increases by about 8 times for every doubling of W. An intuitive explanation is that a wider window allows input samples with various amplitudes to fall into the window and thus leads to greatly increased fluctuation. This fluctuation is considered as "noise" of the estimation process. If the "noise" is large, $s_v^2(\tau)$ will substantially fluctuate from $\sigma_v^2(\tau)$ and it may not accurately represent the timing-skew $|\tau|$. To suppress the fluctuation and ensure an accurate timing-skew calibration, a substantially larger M is needed for a larger W, which reduces the convergence speed significantly.

The value of σ_s^2 can be calculated in the following way. For a single sample captured by the window detector, the fluctuation in its variance is given by $Var(V_{in}^2(t+\tau)|_{f=1})$. Out of M sub-ADC input samples, the number of samples falling inside the window, N_f, can be expressed as:

$$N_f = \sum_{m=1}^{M} f[m] \cong M \cdot P(f = 1) = M \cdot p_0 \cdot W \tag{2.3}$$

where $P(f = 1)$ is the probability of an input falling inside the window,

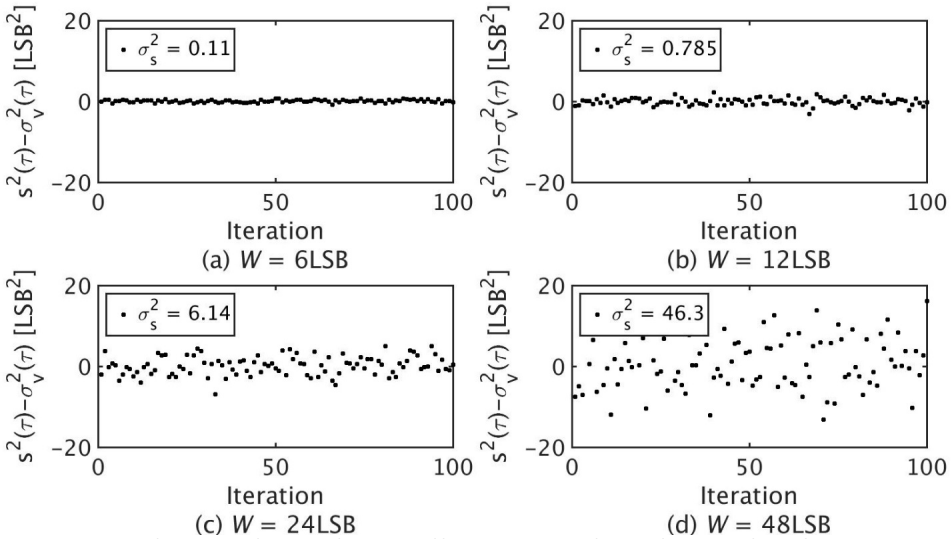

Figure 2.8: Behavioral simulation illustrating the relationship between W and the distribution of $s^2(\tau) - \sigma_v^2(\tau)$, for 100 samples.

and it is given by the product of W and the probability density of V_{in} inside the window, denoted as p_0. For simplicity, V_{in} is assumed to be uniformly distributed within the window [−W, +W] in (2.3), which is valid especially for a small W. Averaging over N_f samples, the fluctuation in the variance estimation is reduced by N_f times and thus σ_s^2 can be computed using the standard statistical analysis as in [31]:

$$\begin{aligned}\sigma_s^2(\tau) &\cong \frac{Var(V_{in}^2(t+\tau)|_{f=1})}{N_f} \\ &\approx \frac{Var(V_{in}+\tau\cdot\frac{dV_{in}}{dt})^2|_{f=1})}{N_f} \approx \frac{\frac{4}{45}W^4+\frac{4}{3}W^2\tau^2\sigma_{dv}^2+2\tau^4\sigma_{dv}^4}{M\cdot p_0\cdot W}\end{aligned} \tag{2.4}$$

Similar to (2.1), the orthogonality of $V_{in}(t)$ and $\frac{dV_{in}}{dt}$ is used to derive (2.4). As shown in (2.4), although N_f linearly increases with W, $Var(V_{in}^2(t+$

$\tau)|_{f=1}$) increases with W^4, and thus, the net effect is that $\sigma_s^2(\tau)$ increases with W^3, which explains the cubic relationship seen in Fig. 2.8. Consequently, a smaller W is preferred to reduce the fluctuation σ_s^2 and increase the convergence speed. Nevertheless, the value of W should not be chosen to be too small. As can be seen from (2.4), if W is decreased until it is much smaller than $\tau \cdot \sigma_{dv}$, then $\sigma_s^2(\tau)$ increases back again because $Var(V_{in}^2(t+\tau)|_{f=1})$ is dominated by $\tau \cdot \sigma_{dv}$ instead of W. Thus, there exists an optimum value for W, which is comparable to $\tau \cdot \sigma_{dv}$.

So far, only the "noise" component in the variance estimation is discussed. In the calibration process, the "signal" component is also critical in determining the convergence speed. This work adopts the min-max search method similar to [18] to minimize the sample variance. Basically, it computes and compares the current sample variance $s_v^2(\tau)$ and its adjacent sample variance $s_v^2(\tau+\tau_{step})$, where τ_{step} is the unit step size of the VDL, as shown in Fig. 2.7 right. If $s_v^2(\tau) < s_v^2(\tau+\tau_{step})$, it implies that $\tau > 0$ and the VDL must be adjusted to decrease τ. On the other hand, if $s_v^2(\tau) > s_v^2(\tau+\tau_{step})$, then $\tau < 0$ and the VDL should be tuned to increase τ. Therefore, the "signal" component that directs the VDL to a smaller $|\tau|$ is the difference between $\sigma_v^2(\tau)$ and $\sigma_v^2(\tau+\tau_s tep)$, which is essentially the derivative of $\sigma_v^2(\tau)$ of (2.1). Thus, the magnitude of "signal" in the estimation process, denoted as $S_{est}(\tau)$, can be computed as,

$$S_{est}(\tau) = \tau_{step} \cdot |\frac{d}{d\tau}\sigma_v^2(\tau)| = 2\tau_{step} \cdot |\tau| \cdot \sigma_{dv}^2 \tag{2.5}$$

$S_{est}(\tau)$ is proportional to τ_{step} because the difference between $\sigma_v^2(\tau)$ and $\sigma_v^2(\tau+\tau_{step})$ increases with τ_{step}. $S_{est}(\tau)$ also increases with $|\tau|$ due to the quadratic dependence of $\sigma_v^2(\tau)$ on τ in (2.1). To ensure a robust calibration, $S_{est}(\tau)$ needs to be larger than the "noise" component in the variance estimation, which is σ_s of (2.4). Otherwise, the random fluctuation in the variance estimation can tune the VDL towards a wrong direction. Combining (2.4) and (2.5), the SNR in the proposed timing skew calibration process quantifies how likely the VDL will move towards a correction and is defined as:

$$\begin{aligned} SNR_{est}(\tau) &= \frac{S_{est}(\tau)}{\sqrt{2}\sigma_s(\tau)} \\ &= \frac{2 \cdot \tau_{step} \cdot |\tau| \cdot \sigma_{dv}^2}{\sqrt{\frac{2}{M \cdot p_0 \cdot W}(\frac{4}{45}W^4 + \frac{4}{3}W^2\tau^2\sigma_{dv}^2 + 2\tau^4\sigma_{dv}^4)}} \end{aligned} \tag{2.6}$$

where the $\sqrt{2}$ term comes from the fact that the "noise" power doubles when subtracting $s_v^2(\tau)$ from $s_v^2(\tau+\tau_{step})$. A large SNR_{est} guarantees that the VDL tuning is on the right direction. For example, if $SNR_{est} = 3$, it means that the "signal" is 3 times greater than the "noise" in the sample variance comparison. Thus, the probability of the VDL making a correct move towards minimizing τ is 99.85%,which is the cumulative distributive function (CDF) 3σ of a normal distribution. By contrast, if $SNR_{est} = 1$, this probability drops to 84%. In other words, the VDL tuning is 16% incorrect, which may cause large residue timing-skew errors. The SNR_{est} can be used as a barometer to check if the value of M is chosen appropriately. For instance, if SNR_{est} is below the target (e.g., < 3), M must be increased. Likewise, if SNR_{est} is

higher than needed, M can be reduced to increase the convergence speed.

Fig. 2.9 plots the simulated relationship between $SNR_{est}(\tau)$ and W of the proposed technique. The same Gaussian random input model is applied and $M = 10^5$ is used. Quantization error is not considered in the simulation for simplicity. The $SNR_{est}(\tau)$ is computed with $\tau = 5ps$ and $\tau_{step} = 1ps$. $SNR_{est}(\tau)$ is maximized at around $W = 1$ LSB. This is because the "noise" component, $\sigma_s^2(\tau)$, is minimized as explained earlier when discussing (2.4). In the prototype ADC, W is set to 1 LSB to maximize $SNR_{est}(\tau)$. With $M = 10^5$ and each ADC channel operating at 200MS/s, this translates to a short calibration step time of only 0.5ms.

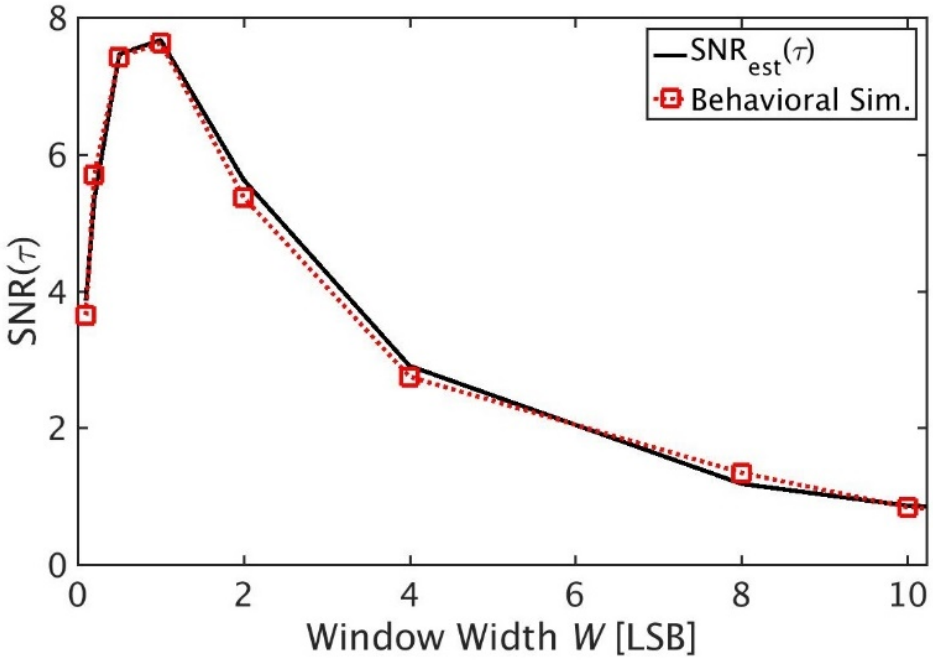

Figure 2.9: Relationship between $SNR_{est}(\tau)$ and W.

According to (2.4), if a wider W is used, M must be increased proportional to W^3 to maintain the same $SNR_{est}(\tau)$. The simulation results with Gaussian random inputs shown in Fig. 2.10 verifies this cubic relationship, analytically derived in (2.4). Behavioral simulation also shows that, the variance-based calibration technique of [22] would require $M = 10^9$ samples to obtain the same $SNR_{est}(\tau)$ as the proposed technique with $W = 1$ LSB and $M = 10^5$, under the same input signal condition.

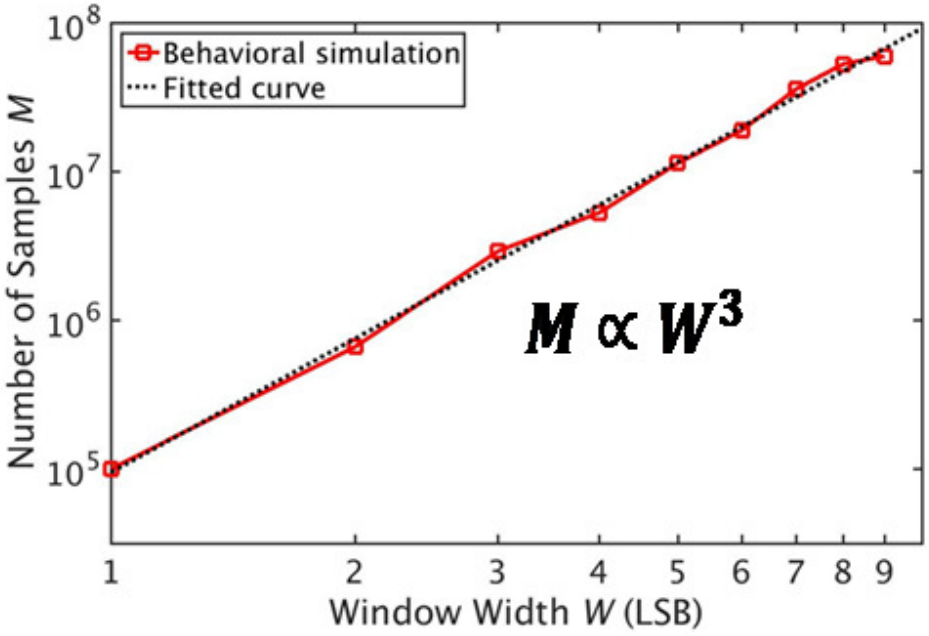

Figure 2.10: Behavioral simulation results illustrating dependence of M on W.

The reason for this significantly longer convergence time is that [22] essentially uses a 4-bit flash ADC as 16 window detectors, whose equivalent window size W is 64 LSB. Thus, the convergence speed ratio of the 16 window

detectors with W of 64 LSB is approximately $64^3/16 = 2^{14} \approx 10^4$. Although [22] does not utilize the actual window detector to collect ADC outputs, it computes variance points over the ADC outputs that are within the range of 64 LSB. Moreover, all ADC outputs are used for the computation and thus, it is equivalent to collecting ADC outputs with 16 window detectors with W of 64 LSB. In addition to a much faster convergence speed, the proposed calibration technique also substantially reduces the power consumption needed for the variation computation. For instance, if the calibration runs full-time to track PVT variations, the calibration digital logics of [22] must run at full-speed since all M ADC samples are used to compute the variance, which may consume a significant amount of power. By contrast, the proposed technique requires only a small number of samples (N_f) falling inside the window. The proposed technique therefore is inactive for most inputs and hence the power consumption can be greatly reduced.

2.4 Effects of Nonidealities and Constraint of the Proposed Calibration Technique

2.4.1 Effect of Thermal Noise

The comparator dominates the input referred noise of both the ADC and the window detector. Assuming the comparator input referred noise is v_n, $\sigma_v^2(\tau)$ can be re-derived as:

$$\begin{aligned} \sigma_v^2(\tau) &= Var(V_{in}(t+\tau) + v_n|_{f=1}) \\ &\cong \sigma_v^2(0) + \tau^2 \cdot \sigma_{dv}^2 + \sigma_n^2 \end{aligned} \tag{2.7}$$

where σ_n is the rms input referred noise of the comparator. The quadratic relationship between $\sigma_v^2(\tau)$ and τ is maintained. Thus, the "signal" component of the proposed calibration technique is unaffected by v_n. The only change is that $\sigma_v^2(\tau)$ is up-shifted by the noise power. The behavioral level simulation results shown in Fig. 2.11 with $1mV$ rms noise confirms the result of (2.7).

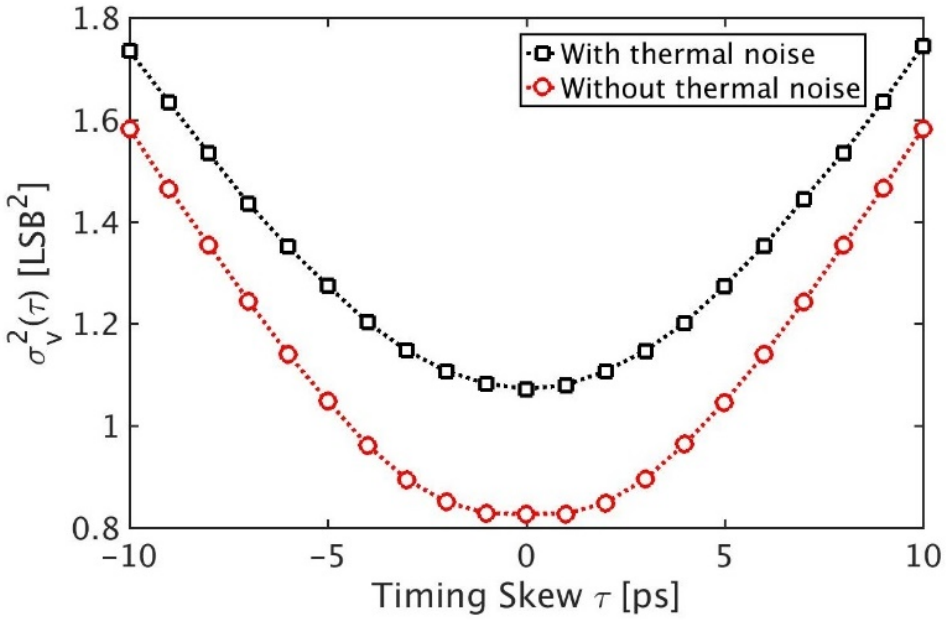

Figure 2.11: Behavioral simulation that illustrates the relationship between variance $\sigma_v^2(\tau)$ and τ with and without thermal noises.

The "noise" component $\sigma_s^2(\tau)$ is re-derived by using the standard statistical calculation:

$$\begin{aligned}\sigma_s^2(\tau) &\approx \frac{Var((V_{in}(t+\tau)+v_n|_{f=1})^2)}{M \cdot P_n(f=1)} \\ &\approx \frac{\frac{4}{45}W^4 + \frac{4}{3}W^2\tau^2\sigma_{dv}^2 + 2\tau^4\sigma_{dv}^4 + \frac{8}{3}W^2\sigma_n^2 + 8\tau^2\sigma_{dv}^2\sigma_n^2 + 8\sigma_n^4}{M \cdot p_0 \cdot W}\end{aligned} \tag{2.8}$$

As expected, the presence of thermal noise increases the fluctuation of the sample variance, degrading $SNR_{est}(\tau)$. Fig. 12 plots $SNR_{est}(\tau)$ versus W with $1mV$ rms noise. Like in Fig. 2.9, quantization error is not considered in this simulation for simplicity. The behavioral simulation results closely track the derived results based on (2.7) and (2.8). Compared to Fig. 2.9 without noise, the $SNR_{est}(\tau)$ in Fig. 2.12 reduces due to increased $\sigma_s(\tau)$. However, it is still greater than 3 with $W = 1$ LSB, and thus, M of 10^5 is still sufficient to ensure the correct timing-skew calibration.

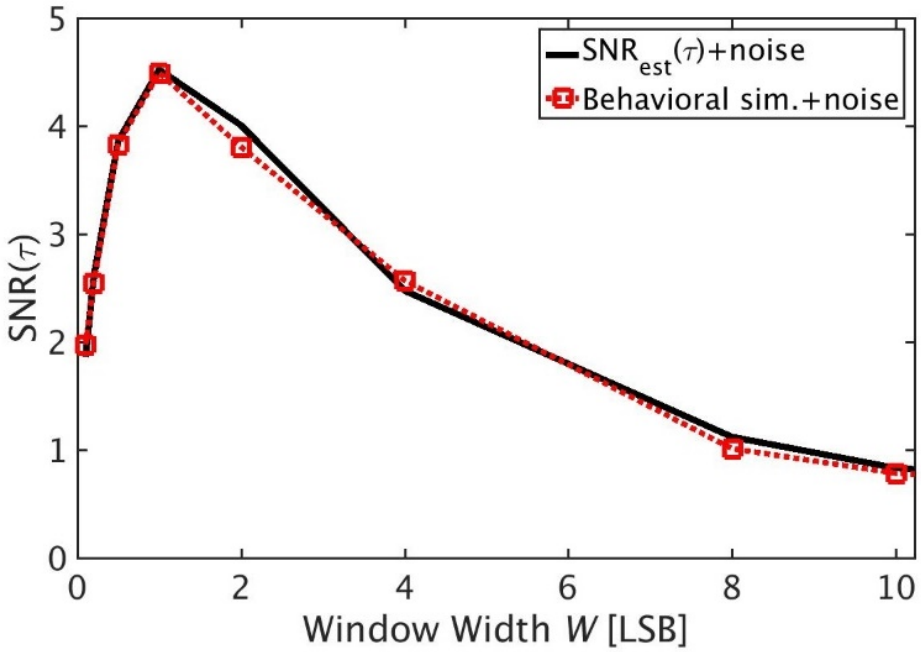

Figure 2.12: Behavioral simulation that illustrates the relationship between $\sigma_v^2(\tau)$ and W with thermal noises.

2.4.2 Effect of Quantization Error

Quantization error can potentially cause errors in the timing-skew calibration if the parameters are not chosen appropriately. For instance, if $W \ll 1$ LSB, $\sigma_n \ll$ LSB, and the timing-skew τ is small, most of ADC inputs falling inside the window are converted to the same digital code, regardless of the exact value of τ Thus, the variance cannot distinguish different τ values, leading to a flat region in the $\sigma_v^2(\tau)$ versus τ curve. Fig. 2.13 shows the behavioral simulation result with $W = 0.25$ LSB and $\sigma_n = 0$. $\sigma_v^2(\tau)$ is flat within τ of $[-1.5ps, 1.5ps]$.

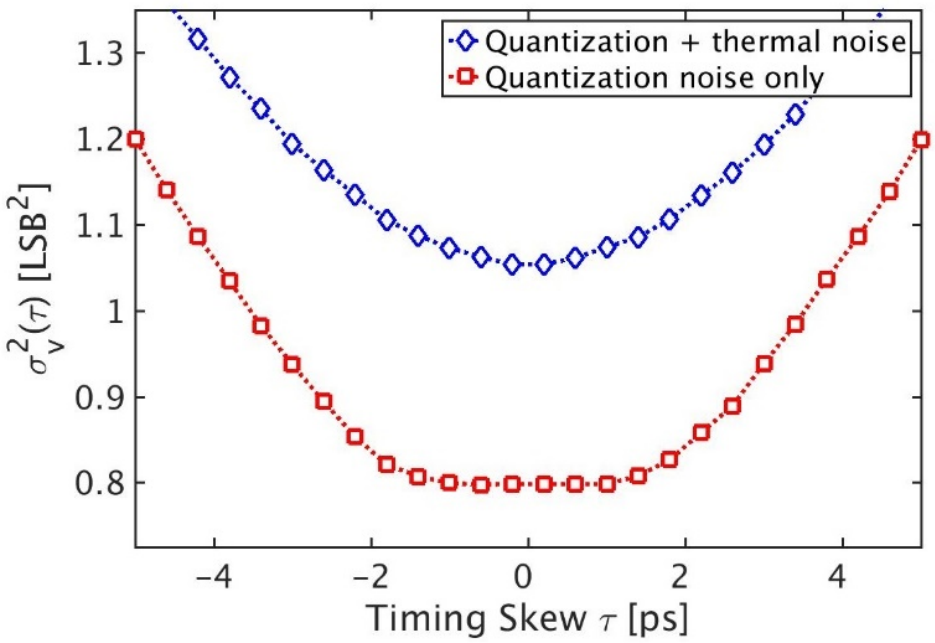

Figure 2.13: Behavioral Simulation illustrates the dead zone and its removal by thermal noise.

Inside this dead zone, the variance estimator cannot determine the direction of the VDL, causing a failure in the timing-skew calibration. Fortunately, this problem can be addressed by the intrinsic thermal noise of the ADC and the window detector. As shown in Fig. 2.14, in the absence of the thermal noise, the ADC input falling inside the window has a narrow distribution, and thus, most of them converts to the same middle code, leading to the dead zone.

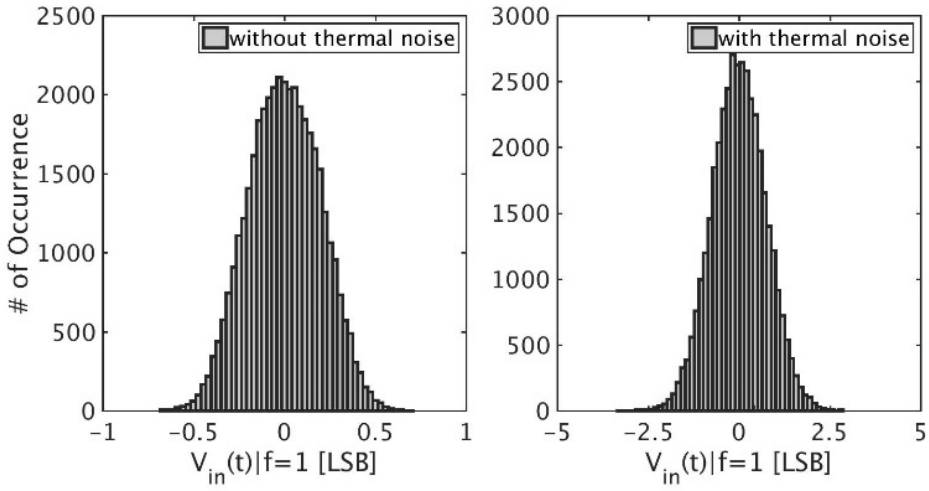

Figure 2.14: Behavioral simulation demonstrates the distribution of $V_{in}(t)|f = 1$ samples with and without thermal noise of $1mV_{rms}$.

By contrast, in the presence of thermal noise $\sigma_n \approx 0.5$ LSB (i.e., $1mV$), the ADC inputs falling inside the window have a much wider spread. Quantization error is effectively linearized by the thermal noise dithering and hence can be considered as a random noise. As a result, the dead zone is removed as shown in Fig. 2.13. Since the ADC thermal noise is usually comparable or bigger than the quantization error in most situations, the effect of quantization error is minor and can be treated just as a slight increase in the overall ADC noise.

2.4.3 Background Tuning of the Window Width

As discussed earlier, the window width W has a strong influence on the convergence time and it is preferred to be set as 1 LSB. Unfortunately, W is sensitive to process, temperature, and voltage (PVT) variations because W

is controlled by the current starved inverter chain delay τ_{delay} (see Fig. 2.2). For this reason, it is necessary to develop a background calibration scheme that enables an accurate tuning of the bias current I_B to ensure W is always equal to 1 LSB, regardless of PVT variations. The key to the background calibration loop is a method to measure W. Since it is nontrivial to sense W directly, W is measured indirectly by monitoring the number of ADC input samples that fall into the window, which is N_f As shown in (2.3), N_f is linearly proportional to W. Since N_f can be easily counted, if the mapping between N_f and W is known a priori, I_B and W can be adjusted to reach the target N_f that corresponds to $W = 1$ LSB. However, the problem of this approach is that the ratio between N_f and W depends on the input signal distribution. For a non-stationary input, the mapping coefficient is unknown and varies with time. To overcome this difficulty, instead of using the unreliable direct mapping between N_f and W, the number of ADC output samples that fall into the digital window of $\{-1, 0, +1\}$ LSB, denoted as N_{ADC}, is monitored. The code of 0 LSB represents the ADC middle code with $V_{in} = 0V$. Since the high-level operation of the ADC is to map an analog input to a digital output with small random perturbations, it is easy to show that a digital window of $[-1, +1]$ LSB at the ADC output corresponds to an analog window of $[-1.5, +1.5]$ LSB at the ADC input, considering the effect of quantization error. Thus, $\frac{N_f}{N_{ADC}} = \frac{2}{3}$ for $W = 1$ LSB, $\frac{N_f}{N_{ADC}} > \frac{2}{3}$ for $W > 1$ LSB, and $\frac{N_f}{N_{ADC}} < \frac{2}{3}$ for $W < 1$ LSB. Note that this relationship is robust and insensitive to the input signal characteristics. The simulation results shown in Fig. 2.15

validate this key observation: regardless of the input signal types (sinusoidal or random) and amplitudes, $\frac{N_f}{N_{ADC}} = \frac{2}{3}$ for $W = 1$ LSB. Thus, by tuning I_B to ensure $\frac{N_f}{N_{ADC}} = \frac{2}{3}$, W can be always kept at 1 LSB, even in the presence of PVT variations.

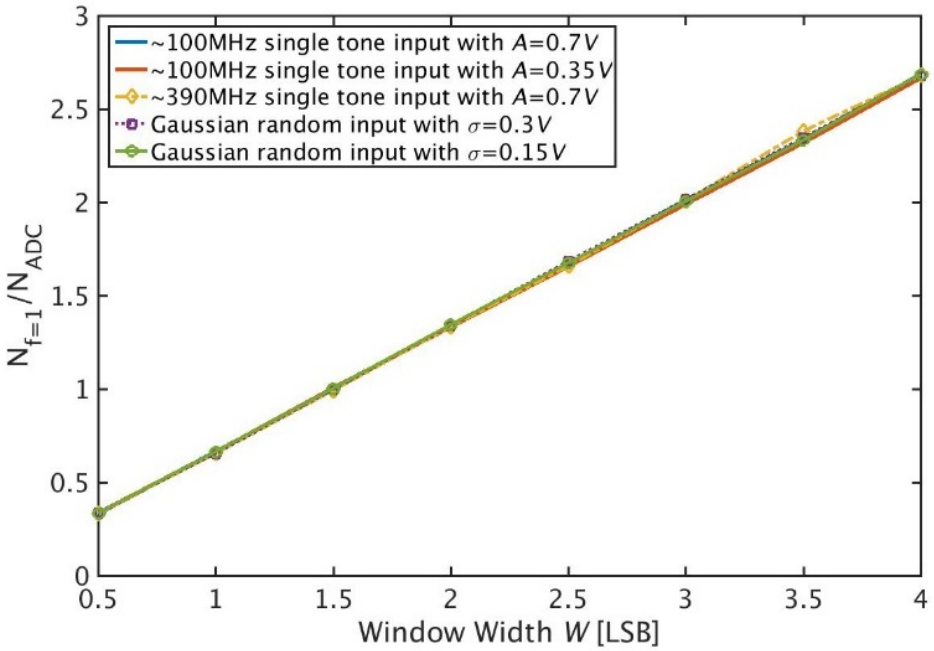

Figure 2.15: Behavioral simulation demonstrates the relationship between $\frac{N_f}{N_{ADC}}$ and the window width W with different inputs.

The unit step size for W calibration (ΔI_B) is determined based on its effect on $SNR_{est}(\tau)$. From (2.6), $SNR_{est}(\tau)$ degrades by almost 10% when W is shifted by 1/2 LSB. Therefore, the unit step is designed to shift W by 1/4 LSB so that the $SNR_{est}(\tau)$ degradation is less than 10% after calibration. Based on the measurement results, approximately, ΔI_B of 70μA shifts W by 1/4 LSB. Considering the full calibration range is from 0 to 5 LSB, 5b of ΔI_B

is sufficient for W calibration. About 10^4 samples are needed for an accurate estimation of $\frac{N_f}{N_{ADC}}$ for each calibration cycle. The total calibration time for W considering all these design matters is still short ($< 100\mu$s).

2.4.4 Practical Limitations of the Proposed Timing Skew Calibration Technique

As in many background timing-skew calibration schemes, the proposed technique has some restrictions on the ADC input signal. It requires the input to have frequent zero crossings to collect enough samples that fall into the window. In addition, the amplitude and frequency of the input signal need to be reasonably large so that the zero-crossing slope $\frac{dV_{in}}{dt}$ is not too small, as otherwise, the influence of the timing skew τ on the sample variance may be too weak, leading to a slow convergence. Furthermore, input frequency (f_{in}) must not be equal to $N \times f_{s,CH}$, where $f_{s,CH}$ is the sampling frequency of single channel and N is an integer number. If f_{in} is equal to $N \times f_{s,CH}$, each ADC channel samples the same input all the time and the variance will be 0. These requirements, however, are not difficult to satisfy in practical applications. As indicated in Fig. 2.7, the proposed technique works well for both sinusoidal signals and wide-band random signals, which cover a wide application space. However, this technique does not work with DC or a pulse wave input, which does not satisfy the above specifications of the input signals.

2.5 Measurement Results

The proposed calibration technique is applied to an 800-MS/s 4-way TI ADC in 40nm CMOS. Fig. 2.16 shows the measured spectrum of the TI ADC before and after using the proposed offset calibration scheme (see Section II-B).

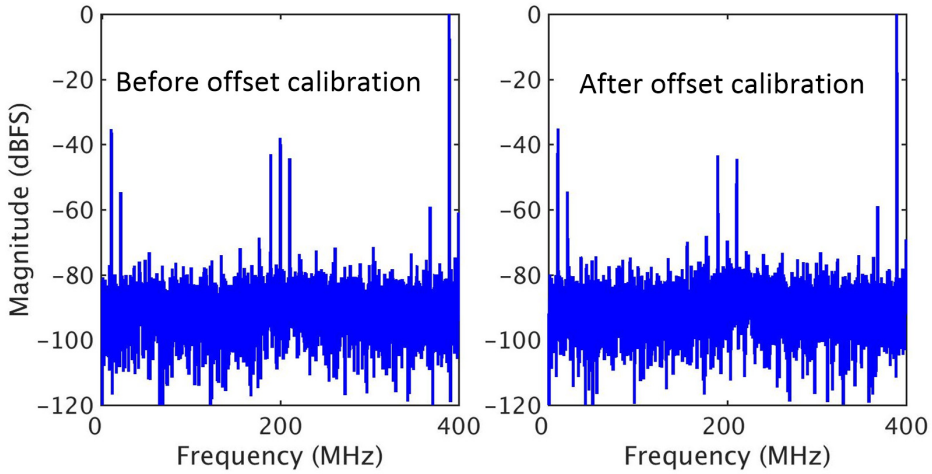

Figure 2.16: Measured spectrum of the TI ADC before (left) and after (right) offset calibration with the proposed technique.

The offset tone at 200 MHz is suppressed from -38 dBFS to -69 dBFS. The CDAC mismatches of all four channels were not impeding the TI-ADC to achieve the targeted linearity of 48dB and thus, no calibration scheme was needed to calibrate CDAC mismatches. The gain mismatch is calibrated in the digital domain. Fig. 2.17 shows the measured spectrum of the TI ADC (left) and a single channel (right) before timing-skew calibration at a low input frequency $f_{in} = 10$ MHz.

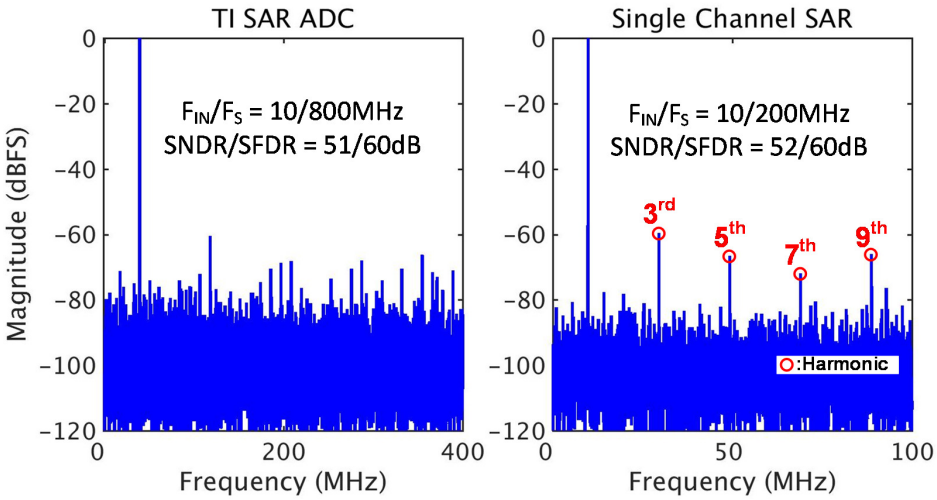

Figure 2.17: Measured spectrum of the TI ADC (left) and a single channel (right) before timing-skew calibration with the input frequency of 10MHz.

The measured SNDR and SFDR of the single-channel ADC are 52 dB and 60 dB, respectively. The tones in the spectrum of the single-channel ADC is noticed to be the odd input harmonics. Timing-skew indicated errors are insignificant and do not limit the TI ADC performance. The measured 51 dB SNDR of the TI ADC is limited by the performance of the single channel ADC. The 1 dB SNDR difference between the single channel ADC and the TI ADC comes from remaining offset and gain mismatches among the 4 ADC channels. Fig. 2.18 shows the measured spectrum of the TI ADC (left) and the single channel (right) before timing-skew calibration with a near Nyquist input $f_{in} = 389$ MHz.

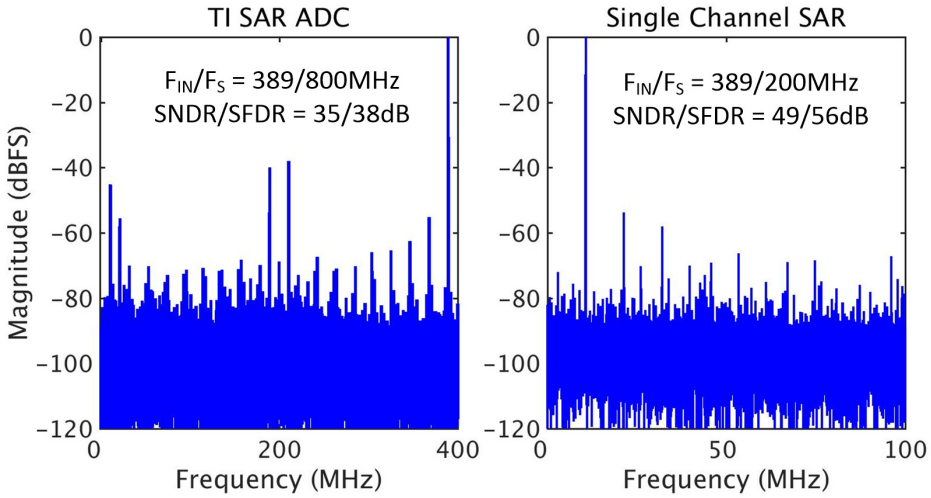

Figure 2.18: Measured spectrum of the TI ADC (left) and a single channel (right) before timing-skew calibration with the Nyquist input at 389MHz.

The measured single-channel ADC SNDR and SFDR are 49 dB and 56 dB, respectively. The 3dB performance degradation compared to the low frequency (see Fig. 2.17, right) is mainly due to increased distortions. The noise floor is almost the same, which indicates that the error due to clock jitter is negligible. The TI ADC SNDR and SFDR at Nyquist are 35 dB and 38 dB, respectively, which are limited by the timing-skew tones. Fig. 2.19 compares the spectrum of the TI ADC with the Nyquist rate input before (left) and after (right) timing-skew calibration. After calibration, the timing skew tones are reduced to below -61 dBFS and the SFDR is limited by the 2^{nd} harmonic of input. The SNDR and SFDR are improved to 48 dB and 56 dB, respectively, which are close to the performance of the single-channel ADC (see Fig. 2.18 right), indicating that channel mismatches have been greatly suppressed.

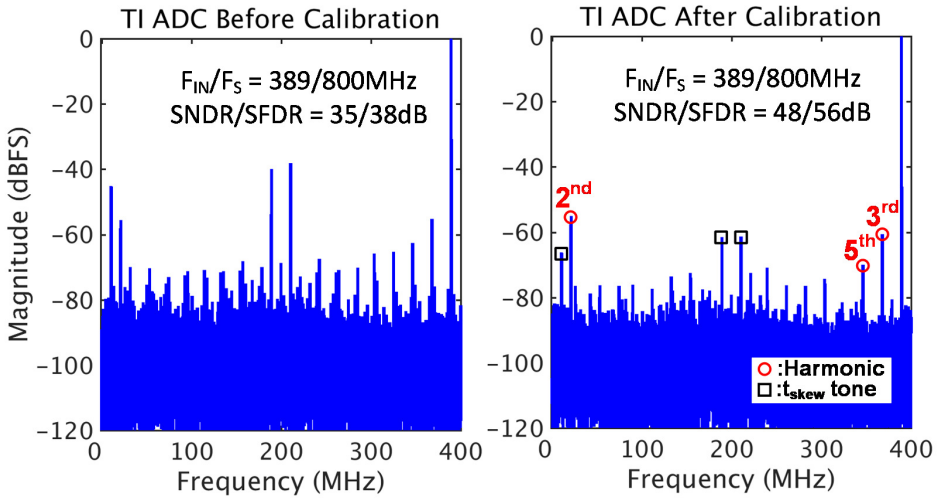

Figure 2.19: Measured spectrum of TI ADC before (left) and after (right) timing-skew calibration with the Nyquist input at 389MHz.

Fig. 2.20 shows that the measured sample variance, s_v^2, as a function of the VDL control code. s_v^2 for each channel reaches its minimum after the proposed timing-skew calibration. The minimum points are positioned at different locations due to random process variations, but only 1 minimum point is observed, and the overall quadratic shape matches the analyses in Section II and III. Fig. 2.21 illustrates the SNDR versus the calibration cycles. 17 cycles are needed to minimize variances of all four channels and the SNDR improves from 42dB to 48.3dB and remains at 48dB for the rest of the cycles.

Fig. 2.22 left shows the measured mean of the sample variance $s_v^2(\tau)$ across 100 times measurements with a full-scale 389-MHz sinusoidal input. As expected, the measurement results match well with $\sigma_v^2(\tau)$ of (2.6). Fig. 2.22 right shows the measured rms fluctuation of the sample variances for $M = 10^4$

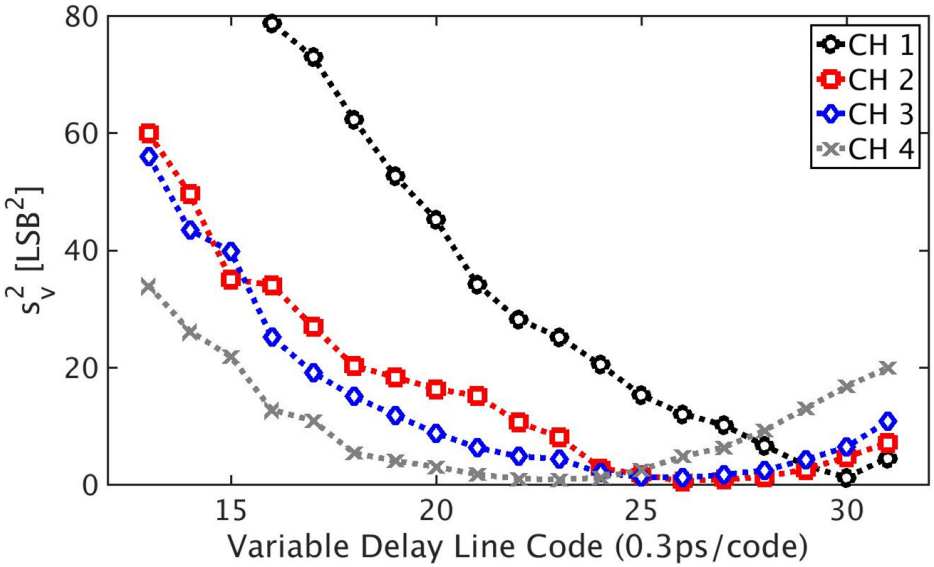

Figure 2.20: Measured variance of inputs falling in the window, s_v^2 versus, VDL control code.

and 10^5. The measurement results also closely track $\sigma_s^2(\tau)$ derived in (2.7), confirming the validity of the theoretical analyses. Measurements also show that, for $M = 10^5$, only about 200 input samples fall into the window and are used to compute the sample variance $s_v^2(\tau)$. Thus, the amount of digital computation and power is much less than that of [21], which requires the variance computation for every sample.

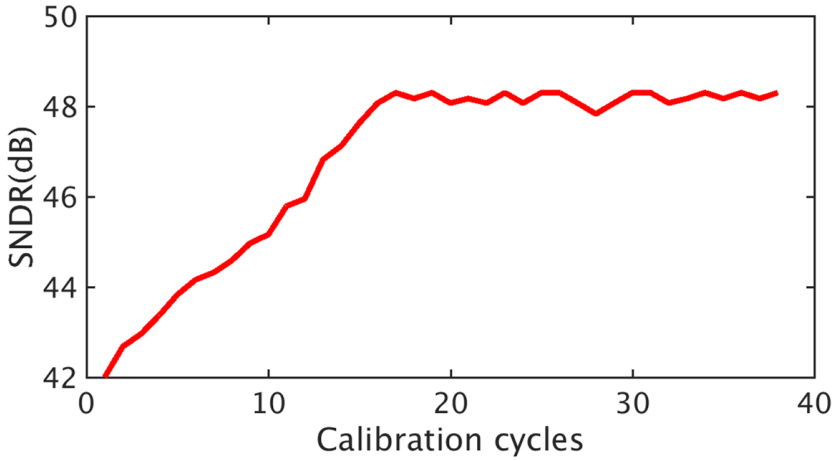

Figure 2.21: Measured SNDR versus calibration cycles

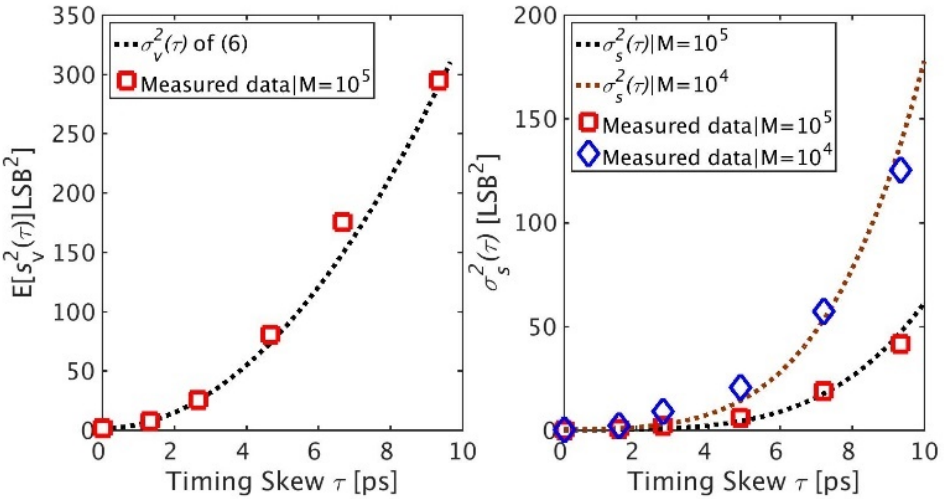

Figure 2.22: Measured mean $E(s_v^2(\tau))$ and fluctuation $\sigma_s^2(\tau)$ of 100 samples of $s_v^2(\tau)$.

Fig. 2.23 shows the measured SNDR versus the ADC input frequency. Before the timing skew calibration, the SNDR decreases monotonically as the input frequency increases. After the proposed timing-skew calibration, the SNDR stays above 48dB across the entire Nyquist band. What limits the

linearity of the TI-ADC is noticed to be the linearity of a single channel. The SNDR/SFDR of the single-channel in Fig. 2.23 closely track those of the TI-ADC after calibration. This also proves that the timing-skew errors are removed and the TI ADC performance is no longer limited by timing skew.

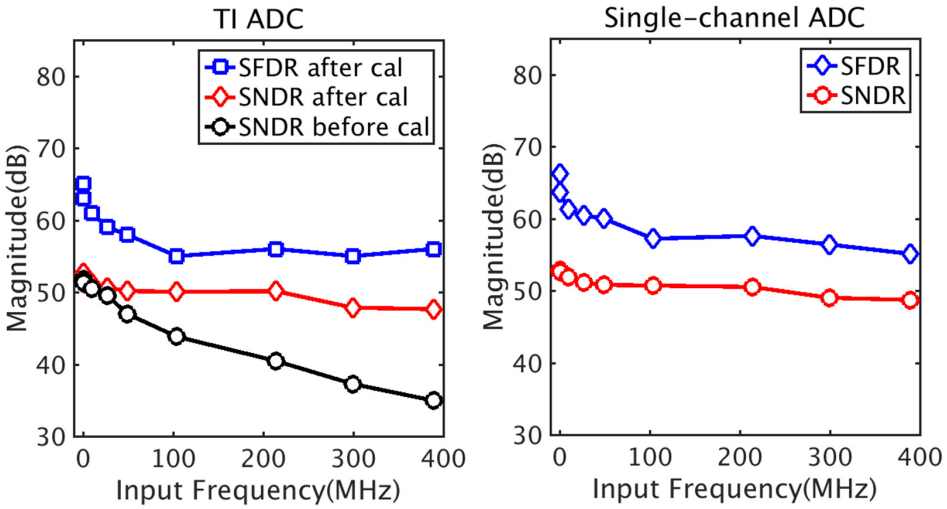

Figure 2.23: Measured SNDR and SFDR versus the input frequency.

Fig. 2.24 shows the measured SNDR versus the input amplitude for three different frequencies. The measured INL and DNL of the TI-ADC and the single-channel ADC are shown in Fig. 2.25. The INL and DNL of the TI-ADC are $+1/-1.5$ LSB and $+0.7/-0.6$ LSB, respectively. The INL and DNL of the single-channel ADC are $+1.7/-1.5$ LSB and $+1.3/-0.9$ LSB, respectively. The INL and DNL of the TI-ADC is slightly improved due to the randomization effect from interleaving multiple channels.

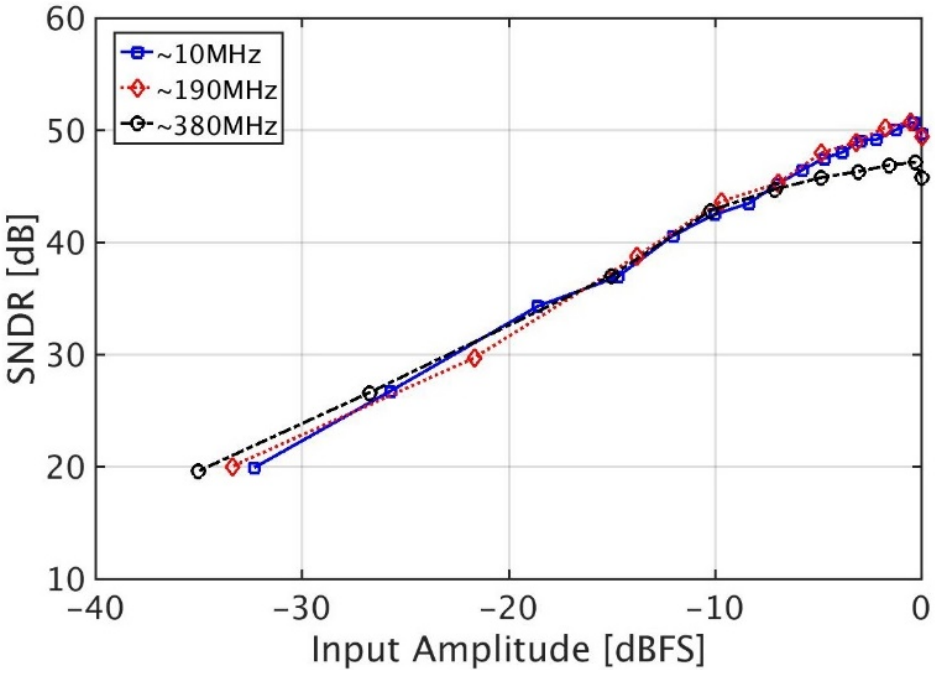

Figure 2.24: Measured SNDR versus the input amplitude with three input frequencies.

Fig. 2.26 shows the chip microphotograph and the active area is $500\mu \times 300\mu$. Clock generator is in the center and the 4 SAR ADCs are symmetrically placed around the clock generator. The window detector is in the right corner of the clock generator and it only occupies a small area compared to the SAR ADC channels.

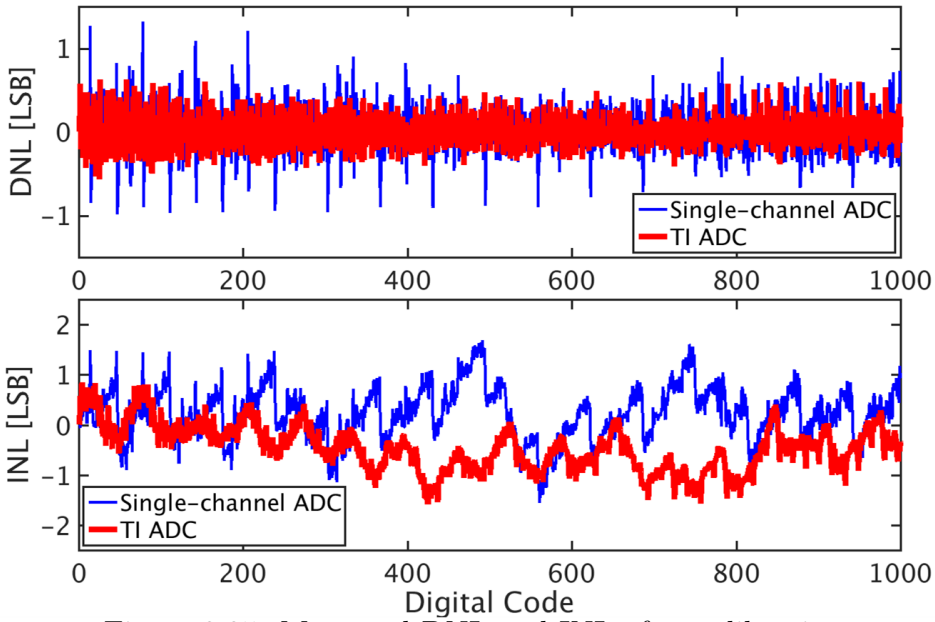

Figure 2.25: Measured DNL and INL after calibration.

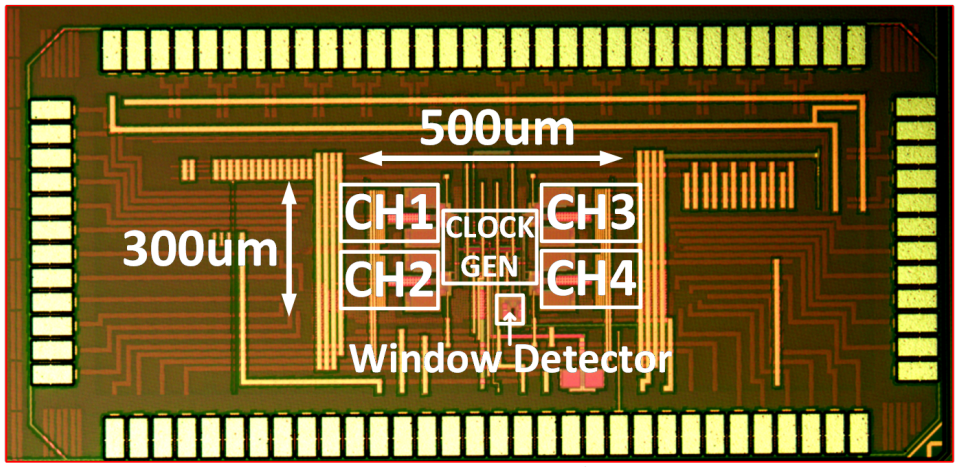

Figure 2.26: Die photo.

The total ADC power is 4.9mW with 1.1V power supply. The power break down at $f_s = 800$ MHz and $V_{DD} = 1.1$V is illustrated in Fig. 2.27. The

SAR and the interleaving digital logic consumes the largest portion of power. The window detector only consumes about 7% of the total power, which proves that its power overhead is small. To estimate the digital hardware cost to compute the variance of ADC outputs, the variance computation hardware is digitally synthesized.

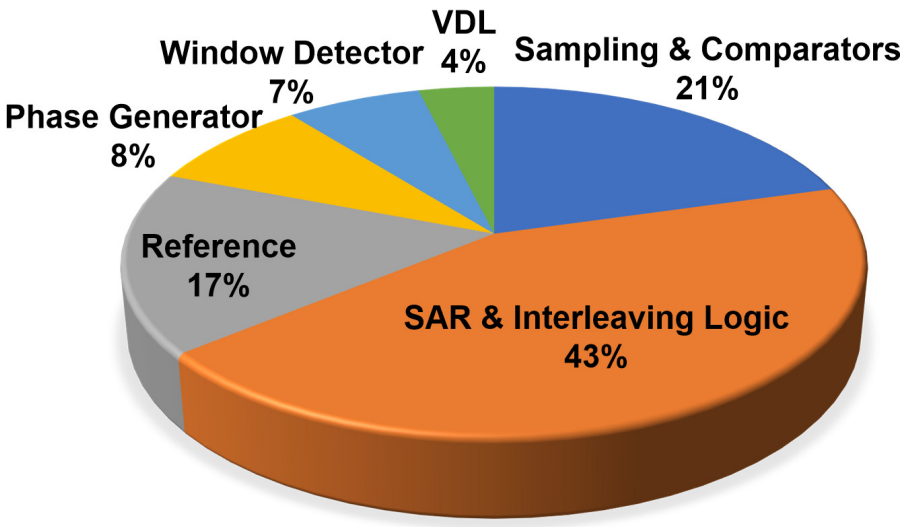

Figure 2.27: Power consumption break down at $f_s = 800\text{MHz}$ and $V_{DD} = 1.1\text{V}$.

One of the key techniques that reduces the power of the proposed work is subtracting the middle code from the collected ADC outputs. Since all the collected ADC outputs are near $[-1, 1]$ LSB, the subtraction leaves only few LSB bits to be active in the hardware and substantially reduces the activity rate as well as the power. Based on the measurement results, where only 200 flags are raised among 10^5 ADC outputs, the hardware is assumed to be active with a frequency of $\approx$ 2MHz and the estimated power consumption is

less than 5% of the total ADC power. Table 2.1 summarizes and compares the estimation techniques and limitations of different calibration methods. Table 2.2 summarizes and compares the performance of this prototype ADC to previously published works with similar speed and resolution. Overall, it achieves a Walden FoM of 29.8fJ/conv-step at the Nyquist frequency, which is comparable to those of the state-of-the-arts.

<table>
<tr><th></th><th>ISSCC '02
Poulton</th><th>ISSCC '10
Greshishchev</th><th>JSSC '11
El-Chammas</th><th>JSSC '13
Stepanovic</th><th>ISSCC '14
Dortz</th><th>JSSC '14
Wei</th><th>JSSC '14
Lee</th><th>This Work</th></tr>
<tr><td>Calibration classification</td><td colspan="2">Foreground
(Require specific input)</td><td colspan="6">Background
(Can work with random input)</td></tr>
<tr><td>Estimation technique</td><td colspan="2">FFT analysis</td><td>Cross correlation-based estimation</td><td colspan="2">Input slope estimation</td><td>Autocorrelation-based estimation</td><td colspan="2">Variance-based estimation</td></tr>
<tr><td>Extra hardware requirements</td><td colspan="2">Test signal generator</td><td>Single comparator reference</td><td>2 full-blown ADCs</td><td>Digital FIR filters</td><td>None</td><td>Flash ADC</td><td>1 window detector</td></tr>
<tr><td rowspan="2">Limitations</td><td colspan="8">Cannot track PVT
Requires sufficiently large dv_{in}/dt, $f_{in} \neq k \times f_{S,CH}$</td></tr>
<tr><td colspan="2">Requires
a signal generator</td><td>Inputs must cross zeros</td><td>Slope estimation heavily depends on f_{in}
Large hardware overhead</td><td>f_{in} is constrained up to $f_s/2$
Power hungry digital FIR filters</td><td>Constraint on shape of input autocorrelation function</td><td>Power hungry Flash ADC</td><td>Inputs must cross zeros</td></tr>
</table>

Table 2.1: Estimation Technique Comparison Summary

Parameters	JSSC '13 Stepanovic	ISSCC '14 Dortz	JSSC '14 Lee	ISSCC '15 Sung	ISSCC '16 Lin	This work
Architecture	TI-SAR	TI-SAR	FATI-SAR	FATI-SAR	TI-SAR	TI-SAR
Technology (nm)	65	40	65	45	40	40
Supply Voltage (V)	1.2	1.1	1	1.1	1.1	1.1
Fs (GS/s)	2.8	1.62	1	1.6	2.6	0.8
Resolution (bit)	11	9	10	10	10	10
Power (mW)	44.6	93	18.9	17.3	18.4	4.9
SNDR @Nyquist (dB)	50	48	51.4	56.1	50.6	48
FoM (fJ/conv-step)	78	283	62.3	21	25.6	29.8
Active Area (mm2)	0.63	0.83	0.78	0.36	0.825	0.15

Table 2.2: Performance Summary

Chapter 3

Mean Absolute Deviation-based Timing-Skew Calibration

This chapter presents a time-interleaved (TI) SAR analog-to-digital converter (ADC) with mean absolute deviation (MAD) based timing-skew calibration technique. To maximize the convergence speed of the timing-skew calibration, a comparator-based window detector (WD) of [34] is utilized to suppress the timing-skew estimation errors and precisely estimate timing skews from orders of magnitude smaller number of samples than those of state-of-the-arts. The proposed calibration technique has low-hardware cost and comparable convergence speed compared to the variance-based timing-skew calibration technique in chapter 2. Moreover, the proposed calibration technique eliminates the needs of squaring operations, which reduced the digital computation power by 50% than the variance-based calibration technique presented in chapter 2. After timing-skew calibration, a prototype 10-b 600-MS/s TI ADC in 40-nm CMOS achieves the peak SNDR of 56dB and 52 dB across the entire Nyquist band. Power consumption is 4.7mW and it leads to the Walden FoM of 23.8-fJ/conversion step.

3.1 Introduction

Time-interleaved (TI) SAR ADC is a well-known energy-efficient ADC architecture for high-speed and medium resolution applications. Without any calibrations, TI-ADC, however, suffers from offset, gain, and timing skew mismatches. Among all mismatches, timing-skew error is the most difficult to calibrate, since it is nontrivial to extract and worsens proportional to the input frequency and amplitude. Existing background timing-skew calibration techniques have different trade-offs among hardware complexity, power and area cost, convergence speed, input-impedance modulation, and restriction on the input signal. [18] requires 2 full-blown reference channels to extract input slope and timing skews of sub-channels. This technique provides a fast convergence speed but it accompanies a large area and power cost. Moreover, the ADC input impedance is periodically varied, which can cause spur and inaccurate calibration. The autocorrelation-based technique of [19] employs only a single comparator as a reference so that it reduces area and power cost. This technique, however, converges slow during background operation with random inputs. To alleviate the area and power trade-offs, calibration techniques without extra hardwares are developed. [33] and [20] do not need any additional channel for calibration, but have tight restrictions on the shape of input autocorrelation function and the frequency range. Furthermore, [20] consumes significant computation power and has a slow convergence speed. Variance-based calibration technique of [22] relaxes the requirement on input signal and does not suffer from input-impedance modulation, but this technique requires

a power-hungry flash and its convergence speed is low. Moreover, every ADC samples are used for the variance-computation, which significantly increases its digital computation power. Although the timing-skew estimation engine can be turned off for most of the time, it needs the PVT-variation detection circuits and increases the hardware complexity of the system. [34] obviates the need for a flash and accelerate the convergence speed by implementing an area and power efficient comparator-based window detector. Moreover, only a fraction of samples (i.e. 200 samples from $M = 10^5$) are needed for timing-skew estimations that significantly reduces the digital power consumption of the estimation engine. This technique, however, still requires power-consuming multiplier due to the squaring operations needed for variance computation.

This chapter presents a novel background timing-skew calibration technique based on mean absolute deviation (MAD). Unlike [7], the proposed MAD technique incorporates a comparator-based window detector (WD), which improves the above-mentioned tradeoffs: first, the proposed technique does not rely on a tight requirement on the shape of the signal's autocorrelation function and its constraint on the input is mild. It only requires the input to have zero crossings and sufficient slope. This constraint is common to many calibration techniques and easily satisfied by many applications; second, although this technique requires a reference channel, its reference is a single comparator-based window detector (WD), which costs low power and area. Furthermore, the WD runs at full ADC rate and thus, the ADC input impedance does not vary; third, its convergence speed is fast. Each calibration cycle requires only

10^5 ADC samples even for random inputs; fourth, its computation is simple because only taking absolute value and averaging are needed. Compared to [34], it does not require any multiplication and only several hundred samples out of 10^5 ADC outputs are used for the actual computation, which substantially reduces the digital power consumption. To verify the proposed calibration technique, a prototype 10-b 600-MS/s TI ADC is built in 40-nm CMOS. After the timing-skew calibration, the peak SNDR of 56dB and 52 dB across the entire Nyquist band is achieved. Power consumption is 4.7mW and it leads to the Walden FoM of 25-fJ/conversion step. The timing-skew estimation engine is digitally synthesized for the power estimation. With the same testbench environment, the proposed MAD-based technique reduced the power consumption to almost half of the power of the variance-based technique.

This chapter is organized as follows. Section 3.2 introduces the proposed timing-skew calibration technique. Section 3.3 presents the convergence time analysis of the proposed technique. Section 3.4 discusses the nonlinearity effect in the proposed calibration technique. Section 3.5 discusses the comparisons of the proposed technique versus the variance-based technique in the second chapter. Last, Measurement results are shown in Section 3.6.

3.2 The MAD-based Timing-skew Calibration

3.2.1 Circuit Implementation

Fig. 3.1 illustrates the block diagram of the 2-way TI SAR ADC with the proposed timing-skew calibration. The proposed TI-ADC is comprised of

2 SAR channels, a WD, a digital multiplexer, and a MAD estimator. Two single-channel SAR ADCs synchronously resolve 10-b with 1-b redundancy at the ADC rate of $\Phi_{1,2}$. The WD acts as a reference channel running at the full ADC rate (Φ_R). The MAD estimator collects needed outputs from the two SAR ADCs, extracts the timing-skew of each SAR channel, and adjusts the variable delay line (VDL) of each channel for skew corrections. The VDL has 6-b binary-weighted digital control code with a unit delay tuning of 300fs and a total correction range of 19ps.

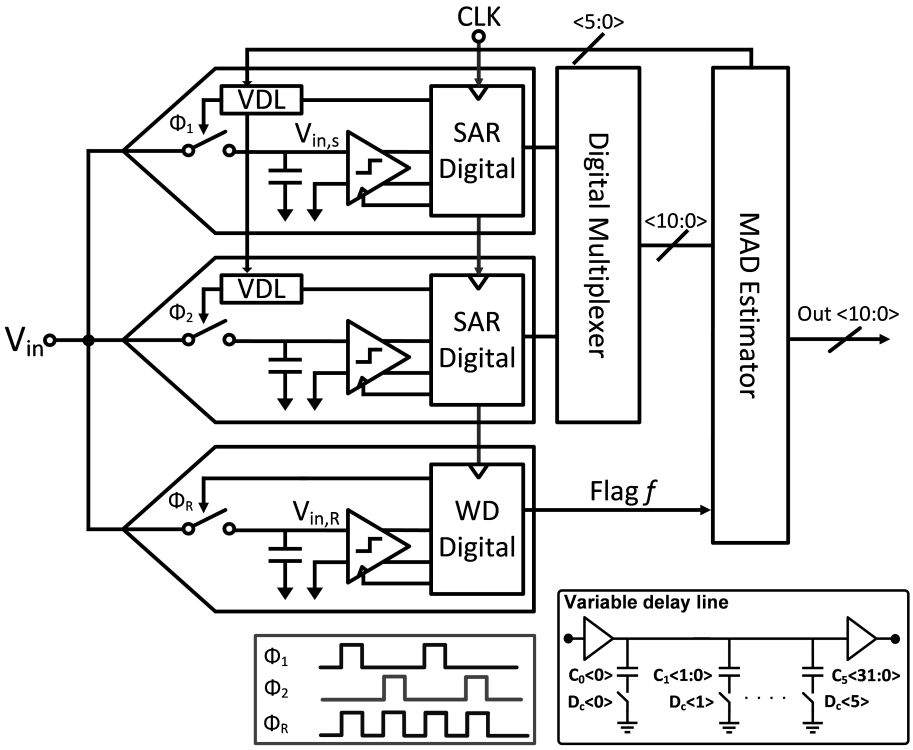

Figure 3.1: Architecture and timing diagram of the proposed 2-way TI-SAR.

Figure 3.2 shows the block diagram of the WD. It is consisted of a

bootstrap switch, a 3-stage comparator, a tunable delay cells, and a DFF that acts as a 1-b TDC that compares the comparator decision time (CDT) with a reference delay. For the proposed calibration technique, the WD identifies if a sampled input $V_{in,R}$, is within a small window W by exploiting CDTs dependence on the input amplitude. If $V_{in,R}$ is near the zero-crossing and falls within [W, +W], the CDT is longer and Φ_{XOR} arrives later than Φ_{delay}, and flag is raised to 1 ($f = 1$). By contrast, if Φ_{XOR} is outside $\pm W$, Φ_{XOR} arrives earlier than Φ_{delay} and flag is not raised ($f = 0$). W is set to 1 LSB to identify samples very close to zero. The choice of W is more thoroughly analyzed in the following sections. Fig. 3.2 also shows the schematic of a 3-stage comparator that is used in both WD and single-channels. When the clock (CLK) is high, the input transistors begin to discharge V_{x1} and V_{x2} nodes that drive the PMOS input pairs of the second stage. When these nodes become sufficiently low, the nodes V_{y1} and V_{y2} get charged toward VDD. When these nodes are sufficiently charged, the third stage starts the regeneration phase. Due to positive feedback from the cross coupled inverters and pre-amplification gains from the first two stages, outputs regenerate quickly. Therefore, the reduced regeneration time allows the SAR ADC to spare more time for DAC settling and SAR logic reconfiguration so that it can satisfy the tight timing-specification of the proposed architecture.

Two SAR ADCs make a full conversion of 10-b with 1-b redundancy in 12 synchronous clock cycles. 11 clock cycles resolve 10-b and 1-b redundancy; and 1 clock cycle is used to sample inputs and reset the SAR logics

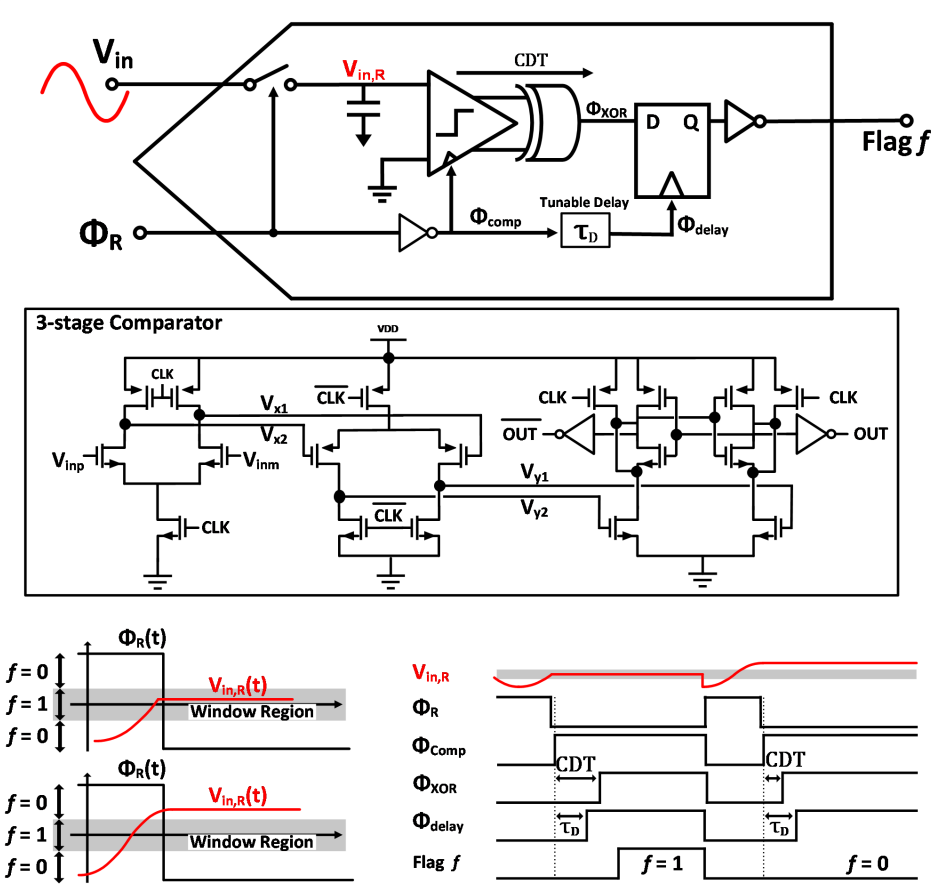

Figure 3.2: Architecture and timing diagram of the proposed window detector.

concurrently. To boost the ADC sampling speed, the DAC settling time is further reduced by implementing the bidirectional single-side switching technique [10], which reduces the total DAC array size by 4 times compared to that of a conventional SAR switching technique. The unit capacitor C is 0.5fF and the total digital-to-analog converter (DAC) capacitance is 272C, including 16C of redundancy. The reduced capacitor DAC array and the 3-stage comparator enable the single channel SAR to achieve the targeted conversion

rate of 300MS/s, where each bit must be fully resolved within $t \approx 278ps$.

3.2.2 Fundamental of the MAD-based Calibration Technique

Figure 3.3 illustrates the principle of the proposed MAD-based calibration technique using a single-tone sinusoidal input as an example. The basic estimation procedure is as follow: first, the WD checks if the sampled input is near the zero-crossing (dark shaded region) and raises the flag ($f = 1$). When the MAD estimation engine detect $f = 1$, it collects the output $D_{out,f=1}$ of the corresponding SAR that has converted the same input that the WD raised the flag. When there is no timing skew, the collected $D_{out,f=1}$ are near 0, where 0 is the middle code and D_{out} spans ± 512. The distribution of the collected $\{D_{out,f=1}\}$ and $\{|D_{out,f=1}|\}$ are shown on the right side of Fig. 3.3. The distribution is very narrow, leading to a small MAD value, $E(|D_{out,f=1}|)$. On the other hand, if timing skew exists, the SAR channel samples inputs before or after the zero crossing, which results in a wider spread of $\{D_{out,f=1}\}$ and $\{|D_{out,f=1}|\}$ distribution (see Fig. 3.3 left), leading to a larger MAD value. Therefore, the MAD value can be basically used as a timing-skew indicator and thus, the timing-skew errors can be removed by monitoring MAD value and adjusting the VDL to minimize it. Moreover, the proposed MAD calibration technique can collaterally calibrate mismatch offset errors as well. When all ADC outputs with $f = 1$ are sorted into the sets of corresponding sub-channels, offset mismatch can be extracted by calculating the mean value of each set. The offset mismatch can be digitally canceled by subtracting from

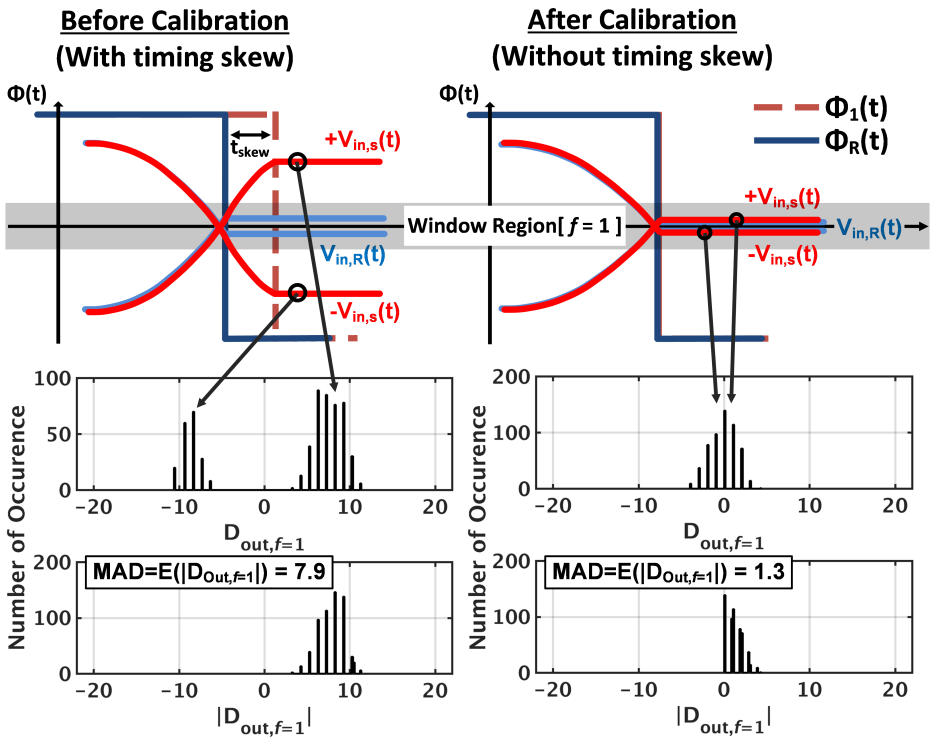

Figure 3.3: The Fundamental idea of the proposed timing-skew estimation technique.

each channel outputs.

3.2.3 Mathematical Derivation and Analysis

To analyze the characteristics of the proposed timing-skew estimation technique, the MAD of the collected ADC outputs with $f = 1$, denoted as $MAD(\tau)$, is derived as follow:

$$\begin{aligned} MAD(\tau) &\equiv E(|V(t+\tau)|_{f=1}|) \\ &\cong \frac{W}{2} erf(\frac{W}{\sqrt{2}\sigma_{dv}|\tau|}) + \frac{\sigma_{dv}^2\tau^2}{2W} erf(\frac{W}{\sqrt{2}\sigma_{dv}|\tau|}) + \frac{\sigma_{dv}|\tau|}{\sqrt{2\pi}} e^{\frac{-W^2}{2\sigma_{dv}^2\tau^2}} \end{aligned} \quad (3.1)$$

where τ is the timing-skew error between the single ADC channel and the WD, W is the size of the window, and σ_{dv} represents the standard deviation of $\frac{dV_{in}}{dt}$ conditioning on $f = 1$. In deriving (3.1), $V_{in}(t)$ and $\frac{dV_{in}}{dt}$ are treated as uncorrelated random variables due to their inherent orthogonality. (3.1) is further simplified based on whether $\sigma_{dv}|\tau|$ is greater or less than W.

$$MAD(\tau) = \begin{cases} \frac{1}{2}W + \frac{\sigma_{dv}^2\tau^2}{2W}, & \sigma_{dv} \cdot |\tau| \ll W \\ \frac{\sigma_{dv}|\tau|}{\sqrt{2\pi}}, & \sigma_{dv} \cdot |\tau| \gg W \end{cases} \tag{3.2}$$

Interestingly, (3.2) reveals that the relationship between $MAD(\tau)$ and τ is different in two cases. When $\sigma_{dv}|\tau|$ is much smaller than W, $MAD(\tau)$ grows quadratically with τ at a rate proportional to σ_{dv}. However, if $\sigma_{dv}|\tau|$ becomes much larger than W, $MAD(\tau)$ increases rather linearly with τ. In Fig. 3.4, the behavioral simulation results with two single-tone sinusoidal inputs (V_{p-p} of 1.1V and f_{in} at 290MHz and 140MHz), two-tone sinusoidal input (V_{p-p} of 1.1V and combined f_{in} of 290MHz and 140MHz), and Gaussian random input with a standard deviation of 0.3V and a bandwidth of [0, 200MHz]. The simulation result with the Gaussian random input is zoomed in to verify the analysis of (3.2). The simulation result with the Gaussian random input closely follows $MAD(\tau)$ of (3.1), which confirms the validity of (3.1) because the result clearly illustrates a quadratic relationship between $MAD(\tau)$ and τ, when τ is less than 4ps, and a linear relationship, when τ is large (i.e. $\tau > 5ps$). In Fig. 3.4, all the behavioral results illustrate that there is only one minimum point exists in the MAD curves; and these minimums are only achieved when τ is close to 0. Therefore, by estimating and minimizing $MAD(\tau)$ towards 0, the timing-skew

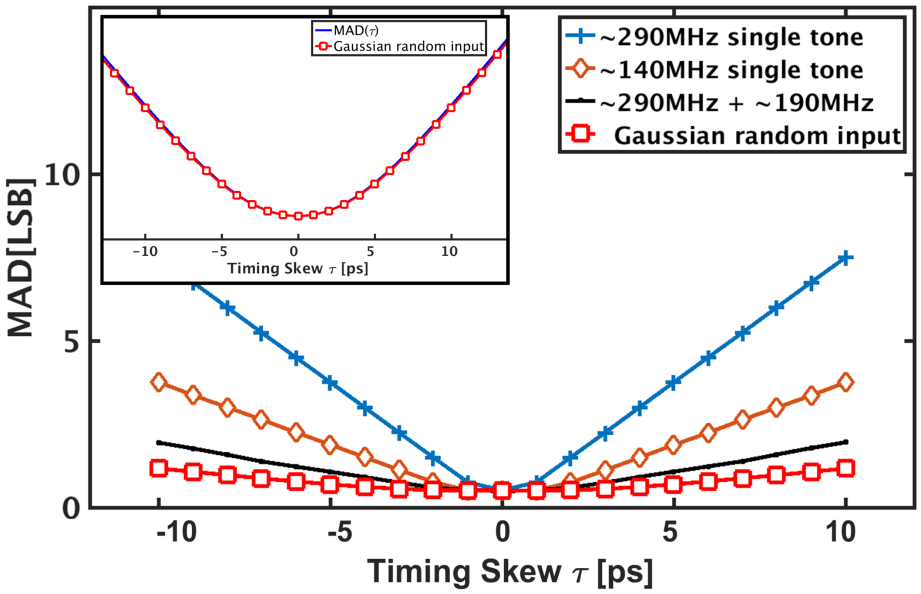

Figure 3.4: The behavioral simulation with sinusoidal inputs illustrating the relationship between $MAD(\tau)$ and τ.

errors can be corrected and this is the fundamental concept of the proposed calibration technique.

3.3 Convergence Time Analysis

Convergence speed is one of the key factors that must be considered in any timing-skew estimation techniques. For the MAD-based estimation technique, its convergence time is limited by the number of ADC outputs M that must be acquired to ensure an accurate estimation of MAD. In this section, an analysis method of the timing-skew estimation accuracy within the context of "signal" to "noise" ratio of the timing-skew estimation, denoted as

SNR_{est}, which is equivalent to that of [34], is presented. This method helps to search the minimum M that maximizes the convergence speed and also satisfies the required MAD-estimation accuracy.

First, for every timing-skew calibration cycle, the sampled MAD, denoted as $s_v(\tau)$, is computed with a limited number of M and it is derived as:

$$s_v(\tau) \equiv \sqrt{\frac{\sum_{m=1}^{M} |V_{in}[m] - V_{avg}| \cdot f[m]}{\sum_{m=1}^{M} f[m]}} \tag{3.3}$$

where V_{avg} represents the sample average, and $f[m]$ is 1 for $|V_{in}[m]| < W$ and 0 for $|V_{in}[m]| > W$. When M approaches to infinity, $s_v(\tau)$ converges to $MAD(\tau)$ of (3.1), although they cannot be equal to each other due to the random nature of inputs. Nevertheless, to ensure that $s_v(\tau)$ is close enough to $MAD(\tau)$ so that $s_v(\tau)$ accurately represent τ, M must be sufficiently large. Among M, the number of samples within the window that is actually used in the computation of $s_v(\tau)$, denoted as N_f, is derived as:

$$N_f = \sum_{m=1}^{M} f[m] \cong M \cdot P(f = 1) \approx M \cdot p_0 \cdot W \tag{3.4}$$

where $P(f = 1)$ is the probability of an input falling inside the window, which is given by the product of W and the probability density of V_{in} inside the window, denoted as p_0. In deriving (3.4), V_{in} is assumed to be uniformly distributed within the window $[W, +W]$, which is valid for small W.

The "noise" of the proposed timing-skew estimation technique is the fluctuation of $s_v(\tau)$ from $MAD(\tau)$. The proposed technique computes and compares the current $s_v(\tau)$ and its adjacent $s_v(\tau + \tau_{step})$, where τ_{step} is the

unit step size of the VDL, to search the the VDL direction to minimize the $s_v(\tau)$, similar to the method of [19]. If the fluctuation is large, $s_v(\tau)$ may not correctly represent τ and the comparison of $s_v(\tau)$ and $s_v(\tau+\tau_{step})$ can possibly mislead the VDL towards a wrong direction. The "noise" of the estimation in $\{s_v(\tau)\}$, denoted as $\sigma_s(\tau)$, is given by $std(|v_{in}(t+\tau)|)$. Averaging over N_f, the fluctuation in the MAD estimation is reduced by N_f times, and thus, $\sigma_s(\tau)$ can be computed using the standard statistical analysis as in [32].

$$\begin{aligned}\sigma_s(\tau) \equiv & \sqrt{\frac{Var(|V_{in}(t+\tau)_{f=1}|)}{N_f}} \\ \equiv & \sqrt{\frac{E[V_{in}^2(t+\tau)] - E^2[|V_{in}(t+\tau)|]}{M \cdot P_0 \cdot W}} \\ \cong & \sqrt{\frac{\frac{1}{3}W^2 + \tau^2\sigma_{dv}^2 - (\frac{1}{4}W^2 + \frac{1}{2}\sigma_{dv}^2\tau^2 + \frac{\sigma_{dv}^4\tau^4}{4W^2})}{M \cdot P_0 \cdot W}}\end{aligned} \tag{3.5}$$

In deriving (3.5), the orthogonality of $V_{in}(t)$ and $\frac{dV_{in}}{dt}$ is also used. Moreover, V_{in} is assumed to be uniformly distributed within $[-W, W]$ for simplicity.

Like [34], the "signal" of the timing-skew estimation, denoted as $S_{est}(\tau)$, directs the VDL towards minimizing $s_v(\tau)$. In order to determine the direction that minimize the MAD, two adjacent sample MADs, $s_v(\tau)$ and $s_v(\tau+\tau_{step})$ are compared, as mentioned above. If $s_v(\tau) < s_v(\tau+\tau_{step})$, it implies that $\tau > 0$ and the VDL must be adjusted to decrease τ. Otherwise, if $s_v(\tau) > s_v(\tau+\tau_{step})$, the VDL must be tuned to increase τ. $S_{est}(\tau)$ is derived as follow:

$$\begin{aligned}S_{est}(\tau) &= \frac{d}{d\tau}E(|V_{in}(t+\tau)|) \cdot \tau_{step} \\ &\cong \frac{\sigma_{dv}^2 \cdot |\tau|}{W} \cdot \tau_{step}, \ |\tau|\sigma_{dv} \ll W\end{aligned} \tag{3.6}$$

$S_{est}(\tau)$ of (3.6) is simplified in condition for $|\tau|\sigma_{dv} \ll W$, since timing skews are much likely to be small. To ensure the VDL to make a correct decision on its direction, S_{est} must be definitely larger than σ_s or "noise" of the estimation. If the estimation "noise" is larger than "signal," the random fluctuation of $s_v(\tau)$ can possibly mislead the VDL towards a wrong direction. Combining (3.5) and (3.6), SNR_{est} can be derived to quantify how likely the VDL will move toward a right direction.

$$\begin{aligned} SNR_{est} &= \frac{S_{est}(\tau)}{\sqrt{2}\sigma_s(\tau)} \\ &\cong \frac{\sigma_{dv}^2|\tau|\tau_{step}}{\sqrt{\frac{2}{M \cdot p_0}(\frac{1}{12}W^3 + \frac{1}{2}\tau^2\sigma_{dv}^2 W - \frac{1}{4W}\sigma_{dv}^4\tau^4)}} \end{aligned} \tag{3.7}$$

where the $\sqrt{2}$ term comes from the fact that the noise power doubles when subtracting $\sigma_s(\tau)$ from $\sigma_s(\tau+\tau_{step})$. A large SNR_{est} indicate that the VDL will much likely adjusted towards the right direction. For instance, if $SNR_{est} = 3$, it indicates that two adjacent $s_v(\tau)$ and $s_v(\tau + \tau_{step})$ are far apart more than three times $\sqrt{2}\sigma_s(\tau)$. Since the two points are farther than 3σ, the VDL will move towards minimizing τ with probability of 99.85%, which is the cumulative distributive function 3σ of a normal distribution. By contrast, if $SNR_{est} = 1$, the probability drops to 84%. In other words, the VDL tuning can make incorrect decisions with 16% chance, which may cause large residue timing-skew errors. Thus, the SNR_{est} can be utilized to check if appropriate number of M is collected for the accurate estimation. For instance, if SNR_{est} is below the target ($e.g., < 3$), M must be increased. Likewise, if SNR_{est} is higher than needed, M can be reduced to increase the convergence speed.

Fig. 3.5 illustrates the relationship between SNR_{est} and W, S_{est} and W, and $\sigma_s(\tau)$ and W. The same Gaussian random input, $M = 10^5$, and τ_{step} of 1ps are applied. The results indicate that the maximum SNR_{est} is achieved when $W \approx 1LSB$.

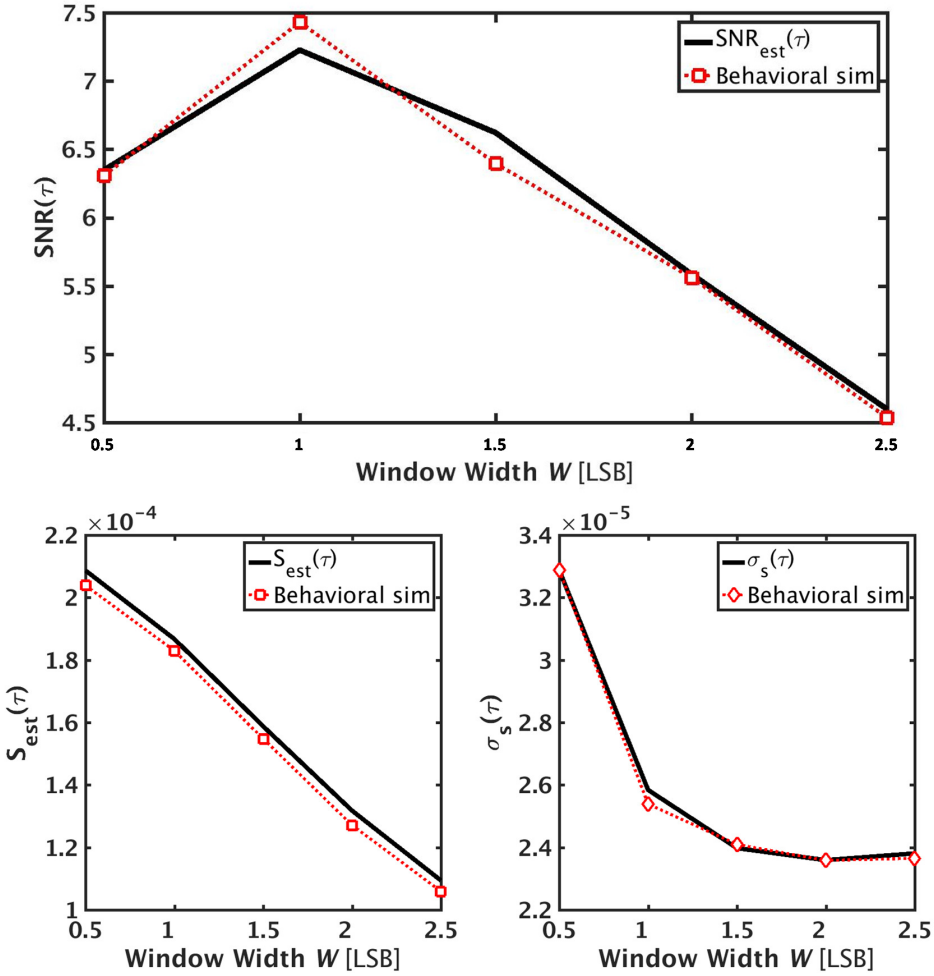

Figure 3.5: Relationship between $SNR_{est}(\tau)$ and W (top) and Relationship between $S_{est}(\tau)$ and W (left) and $\sigma_s(\tau)$ and W (bottom)

That optimum SNR_{est} is found near $W \approx 1LSB$ can be explained

with separate plots of $S_{est}(\tau)$ (bottom left) and $\sigma_s(\tau)$ (bottom right). Fig. 3.5 (bottom right) illustrates an inverse square root relationship between $\sigma_s(\tau)$ and W. On the other hand, in Fig. 3.5 (bottom left), $S_{est}(\tau)$ is noticed to be inversely proportional to W, as derived in (3.6). When W becomes larger than 1LSB, the decreasing rate of $S_{est}(\tau)$ surpasses that of $\sigma_s(\tau)$, since the derivative of $\sigma_s(\tau)$ becomes noticeably small as W passes 1LSB. Therefore, when the rate of change of both $S_{est}(\tau)$ and $\sigma_s(\tau)$ are considered, the optimum SNR_{est} is achieved with W near 1LSB.

The relationship of M and W is analyzed to understand how W affects the convergence speed of the proposed calibration technique. According to (3.7), if a wider W is used, M must be increased proportional to W^3 to maintain the same SNR_{est}. Figure 3.6 confirms the analysis of the cubic relationship of M and W. The same Gaussian random input is applied to the behavioral model. The results show how large M must be increased to maintain SNR_{est} of 3, when W is varied from 1LSB to 5LSB. Then, the result is compared to the linear curve-fit line to verify that indeed $M \propto W^3$. Therefore, the simulation results prove that the optimum convergence speed can be achieved, when W is set to near 1LSB.

3.4 Effect of Nonlinearity

3.4.1 Thermal Noise

The comparator noise dominates the input referred noise of both SAR ADC and the WD. Assuming the comparator input referred noise is v_n, $MAD(\tau)$

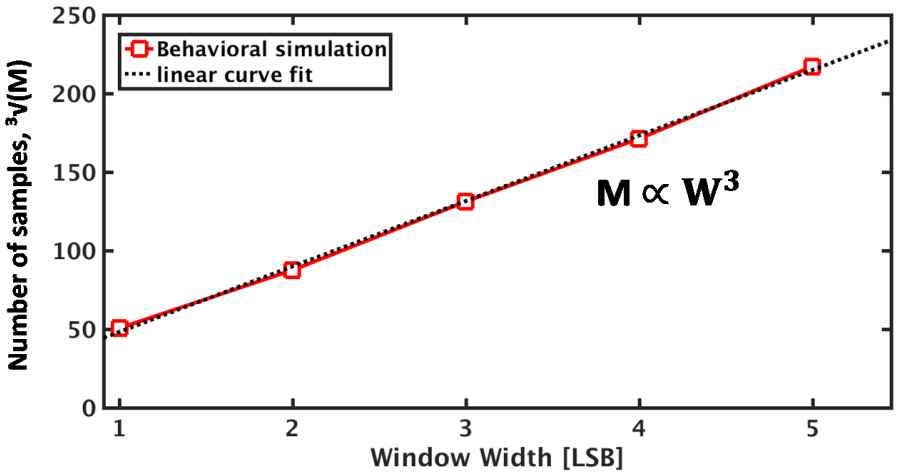

Figure 3.6: Relationship between M and W.

can be re-derived as

$$MAD(\tau) = \begin{cases} \frac{1}{2}W + \frac{\sigma_{dv}^2\tau^2}{2W} + \frac{v_n^2}{2W}, & \sigma_{dv}|\tau| \gg W \\ \sqrt{\frac{\sigma_{dv}^2\tau^2 + v_n^2}{2\pi}}, & \sigma_{dv}|\tau| \gg W \end{cases} \tag{3.8}$$

where σ_n is the rms input referred noise of the comparator. (3.8) shows that the overall relationship between $\sigma_s(\tau)$ and τ remains the same even with the thermal noise. The overall $MAD(\tau)$, however, is increased due to thermal noise effect. The behavioral simulation with 1 mV rms is performed and the result is shown in Fig. 3.7. The overall relationship between $MAD(\tau)$ and τ is conserved. The $MAD(\tau)$, however, has shifted upward as expected due to the thermal noise, which confirms the validity of (3.8).

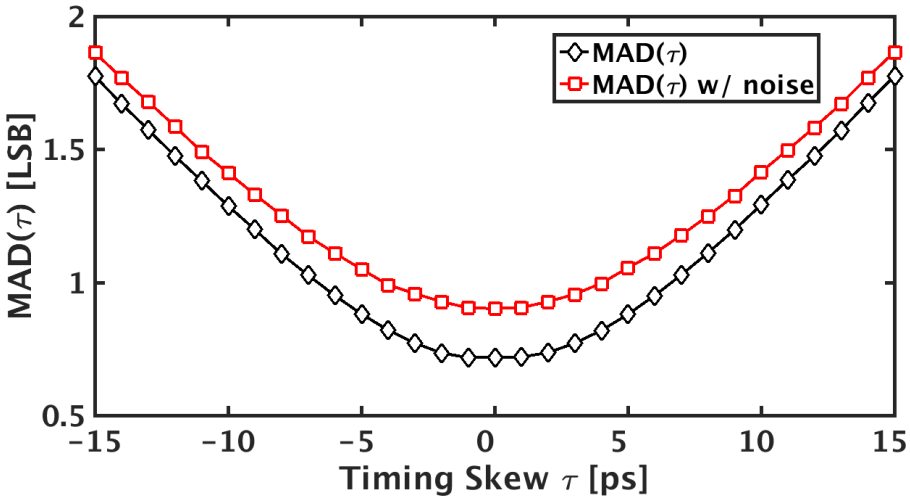

Figure 3.7: The behavioral simulation verifying the quadratic and linear relationship between $MAD(\tau)$ and τ with and without thermal noise.

$\sigma_s(\tau)$ is also re-derived to include thermal noise effect:

$$\begin{aligned}\sigma_s(\tau) &\cong \sqrt{\frac{Var(|V_{in}(t+\tau)+v_n|_{f=1}|)}{N_f}} \\ &\cong \sqrt{\frac{\frac{1}{12}W+\frac{1}{2W}(\tau^2\sigma_{dv}^2+\sigma_n^2)-\frac{1}{4W^3}(\sigma_{dv}^2\tau^2+\sigma_n^2)^2}{M\cdot p_0}}\end{aligned} \tag{3.9}$$

Likewise, the overall relationship between $\sigma_s(\tau)$ and τ is conserved, although the presence of thermal noise increases the overall magnitude of $\sigma_s(\tau)$. It is shown in Fig. 3.8 that the increased $\sigma_s(\tau)$ degrades the $SNR_{est}(\tau)$, when compared to $SNR_{est}(\tau)$ of Fig. 3.5 without noise. The $SNR_{est}(\tau)$, however, is still greater than three with $M = 10^5$, which indicates that the number of collected samples is still sufficient enough to ensure an accurate timing-skew calibration.

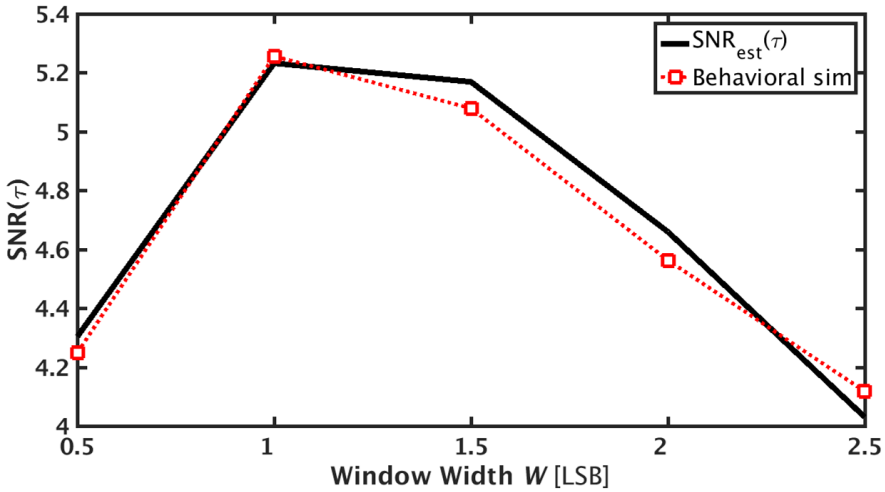

Figure 3.8: Behavioral simulation that illustrates the relationship between $SNR_{est}est(\tau)$ and W with thermal noises.

3.4.2 Practical Limitations of the Proposed Timing-skew Calibration Technique

Like any timing-skew calibration techniques, the proposed MAD-based timing-skew estimation has some restrictions on its ADC input signals. First, since this technique also utilizes the WD for the timing-skew estimation, it requires its inputs to fall into the window and therefore, the inputs must have frequent zero-crossings. Moreover, the amplitude and frequency of the input must be sufficiently large so that the timing skew information is considerable. Last, input frequency (f_{in}) must not be equal to $N \times f_{S,CH}$,where $f_{S,CH}$ is the sampling frequency of single channel and N is an integer number. If f_{in} is equal to $N \times f_{S,CH}$, each sub-ADC samples the same input all the time and the MAD of the collected outputs will be 0. These requirements, however, are satisfied in many practical applications. For instance, the proposed technique

works well for both sinusoidal signals and wideband random signals. This technique, However, does not work with dc or a pulse wave input, which does not satisfy the above specifications of the input signals.

3.5 MAD versus Variance-based Calibration Technique

3.5.1 SNR_{est} of the timing-skew calibration technique

Fig. 3.9 illustrates the behavioral simulation result and the SNR_{est} of the proposed MAD-based calibration technique and the variance-based calibration technique of [34]. The comparison is done within the same test environment and Gaussian random input is applied. Within the W range of $[0.5, 5]$ LSB, the SNR_{est} of the MAD-based calibration technique is noticed to be slightly lower than that of the variance-based technique. In order to understand what makes SNR_{est} of the MAD-based technique slightly lower, SNR_{est} of the two calibration techniques are compared. The SNR_{est} of the variance-based calibration technique of [34], denoted as $SNR_{est,var}$ is shown below.

$$SNR_{est,var} = \frac{\tau_{step}|\tau|\sigma_{dv}^2}{\sqrt{\frac{2}{M \cdot p_0} \cdot (\frac{1}{45}W^3 + \frac{1}{3}W\sigma_{dv}^2\tau^2 + \frac{1}{2w}\tau^4\sigma_{dv}^4)}} \tag{3.10}$$

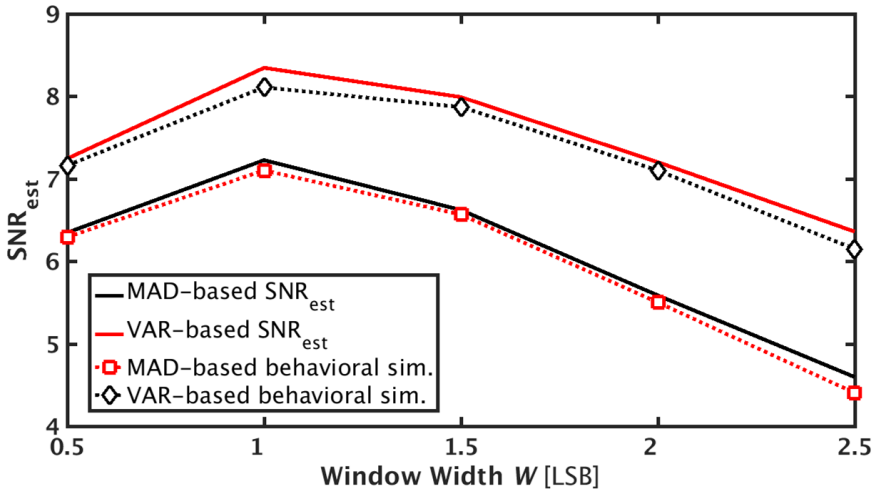

Figure 3.9: SNR_{est} comparison of MAD-based and variance-based timing-skew calibration technique.

For comparison, the nominators of SNR_{est} of both techniques are set equal. Then, when the denominator of the $SNR_{est,var}$ is compared to that of the SNR_{est} of (3.7), it is noticed that $SNR_{est,var}$ has a smaller "noise" contribution by the term with W only. For instance, when $\tau = 0$, the denominator ("noise" of the estimation) of the $SNR_{est,var}$ is equal to $\sqrt{\frac{2}{M \cdot p_0}(\frac{1}{45}W^3)}$, which is approximately 4 times smaller than $\sqrt{\frac{2}{M \cdot p_0}(\frac{1}{12}W^3)}$ of the MAD-based calibration technique. In other words, even though the same sized window is used, "noise" contribution by W is almost four times larger than that of the variance-based estimation. Thus, the MAD-based estimation "noise" is slightly worse and it slightly shifts SNR_{est} downward. The overall relationship between SNR_{est} and W, however, is almost the same for both techniques as shown in Fig. 3.9. Although SNR_{est} of the proposed technique is slightly lower than $SNR_{est,var}$ with the same M, the digital computation power of the

proposed technique is much lower than that of the variance-based technique of [34] due to the elimination of squaring operations. For the fair power comparison, the simulation is performed with the digitally synthesized blocks of MAD-based and variance-based estimation engine. With the same test-case inputs and other variables remain the same, the proposed calibration technique consumed almost 50% less power than that of the [34].

3.5.2 The relationship between M and W

It is interesting to notice that the cubic relationship of M and W illustrated in Fig. 3.6 is also seen in the variance-based calibration technique of [34]. The estimation "noise" of the variance-based technique increases proportional to W^3, whereas the estimation "signal" is not affected by W. In the proposed MAD-based calibration technique, both the estimation "signal" and "noise" are affected by W, as shown in Fig. 3.5. Therefore, although the calibration technique of [34] and the proposed technique yield the same cubic relationship between M and W, an intrinsic difference exists in their derivations.

3.6 Measurement Results

The proposed calibration technique is applied to an 600-MS/s 2-way TI ADC in 40nm CMOS prototype and its die photo is shown in Fig 3.10. Fig. 3.11 shows the measured spectrum of the TI-ADC and the single channel before timing-skew calibration with the input frequency of 1MHz. Timing-

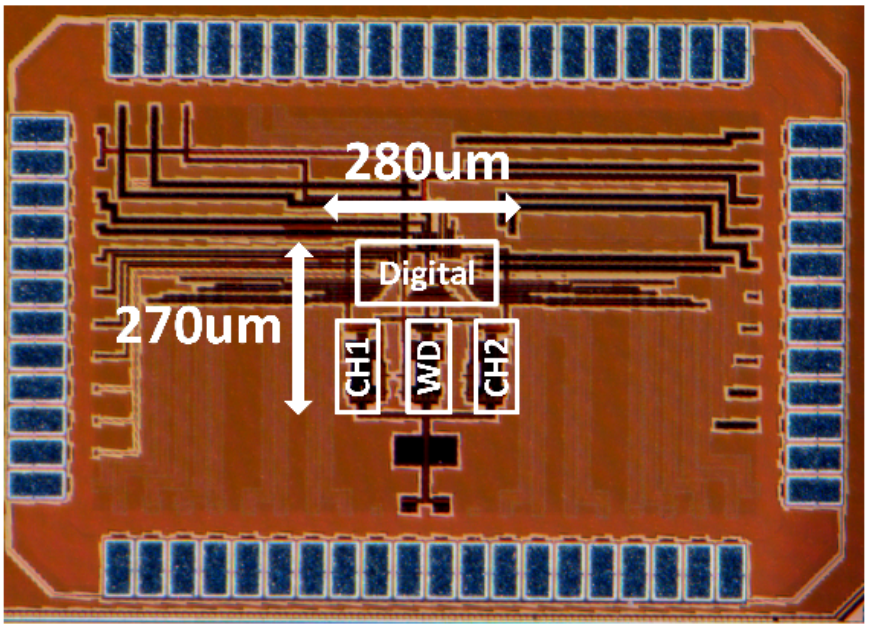

Figure 3.10: Die photo.

skew indicated errors, however, are insignificant and do not limit the TI-ADC performance.The measured 56-dB SNDR of the TI ADC is limited by the performance of the single-channel ADC.

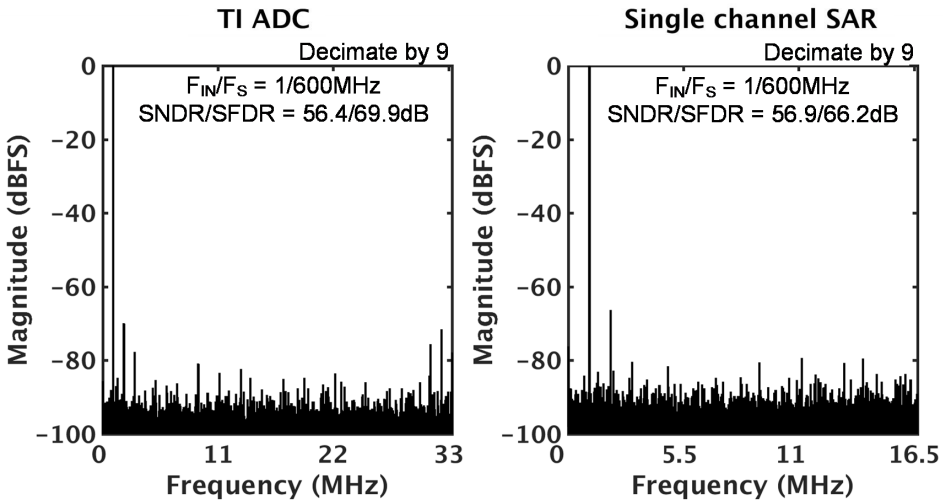

Figure 3.11: Measured spectrum of the (Left) TI-ADC and a (Right) single-channel before timing-skew calibration with the input frequency of 1 MHz

Fig. 3.12 shows the measured spectrum of the TI ADC (left) and the single channel (right) before timing-skew calibration with a near Nyquist input f_{in} of 295 MHz. The measured single-channel ADC SNDR and SFDR are 52 and 57 dB, respectively. The 4 dB performance degradation compared to the low frequency spectrum is mainly due to increased harmonic distortions. The noise floor of the spectrum remains almost the same, which indicates that the errors from random clock jitter is negligible. The SNDR and SFDR of the TI-ADC at Nyquist are 35 and 38 dB, respectively, which are limited by the timing-skew tones.

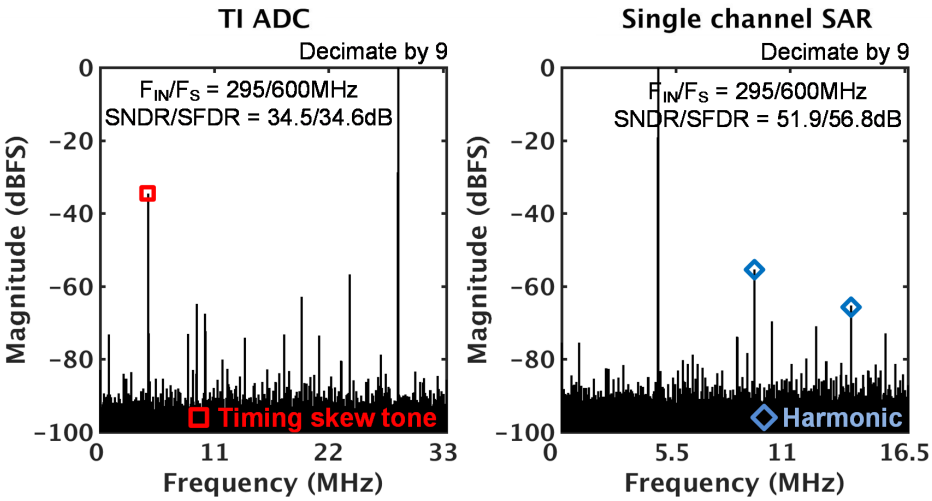

Figure 3.12: Measured spectrum of the (Left) TI-ADC and a (Right) single channel before timing-skew calibration with the Nyquist input at 295 MHz.

Fig. 3.13 illustrates the spectrum of the TI-ADC with the Nyquist rate input f_{in} of 295 MHz before (left) and after (right) timing-skew calibration. Before the calibration, timing-skew tones limit the linearity performance of the TI-ADC. After calibration, the timing-skew tones are reduced to below -75 dBFS and the SFDR is limited by input harmonics. The SNDR and SFDR improves to 52 and 57 dB, respectively.

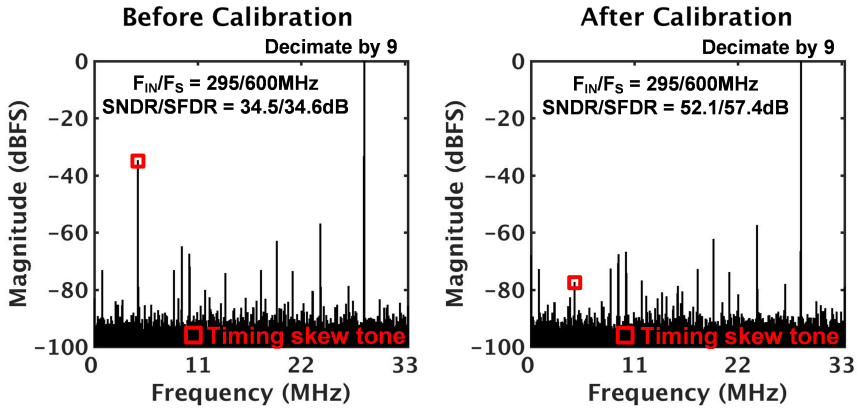

Figure 3.13: Measured spectrum of TI-ADC (Left) before and (Right) after timing-skew calibration with the Nyquist input at 295 MHz.

Fig. 3.14 illustrates the SNDR versus the input frequencies within Nyquist range. Before the timing-skew calibration, the SNDR and SFDR of the TI-ADC are limited by timing-skew errors, which monotonically aggravates with input frequency. After the timing-skew calibration, the timing-skew errors are eliminated and the SNDR and SFDR of the TI-ADC are limited by the performance of single-channel ADC. The SNDR of TI-ADC remains above 52dB across the entire Nyquist band. Fig. 3.15 shows the measured SNDR versus the input amplitude for three different frequencies and Fig. 3.16 illustrates the measured DNL and INL of the TI-ADC.

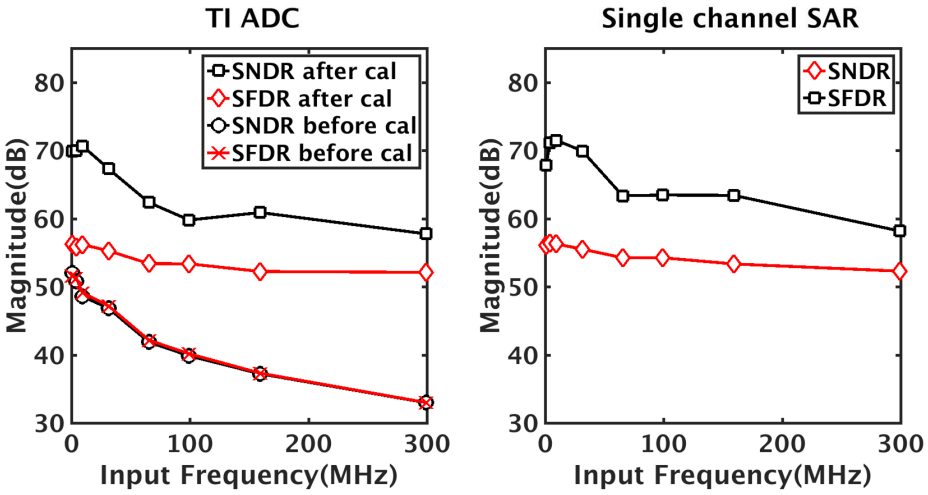

Figure 3.14: Measured SNDR and SFDR versus the input frequency of TI ADC and a single channel.

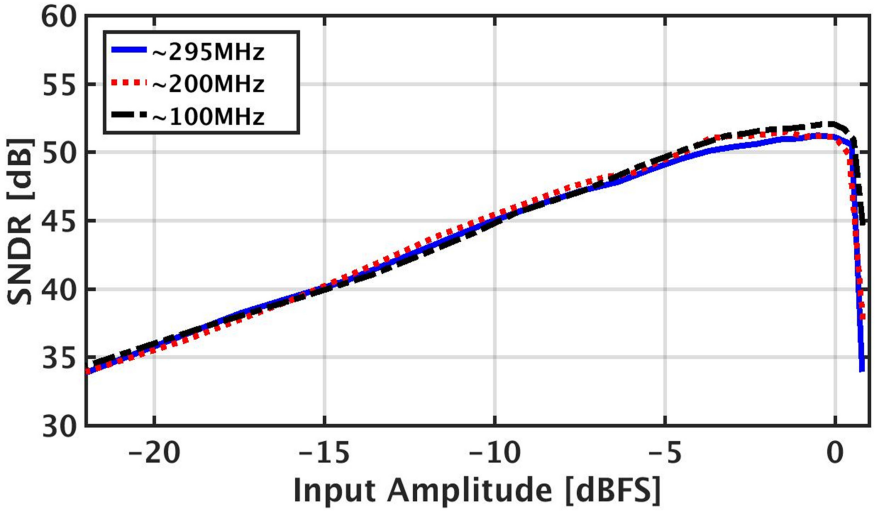

Figure 3.15: Measured SNDR versus input amplitude.

Fig. 3.17 illustrates the SNDR versus the calibration cycles. Thirty cycles, which is equivalent to 6.4ms with F_S = 600MS/s and M=128K, are used to minimize the MAD of all channels, and the SNDR improves from

33 to 52 dB; and it remains at 52 dB for the rest of the cycles. Fig. 3.18 shows the measured sample MAD $s_v(\tau)$ as a function of the VDL control code, when a fullscale 295-MHz single-tone sinusoidal input is applied. $s_v(\tau)$ of both channels reach to their minimums after applying the proposed timing-skew calibration. Due to random process variations, the minimum points are located at different positions but only 1 minimum point is noticed for each channel. A quadratic relationship is noticed near the minimum and a linear relationship is found when the VDL code is far from the minimum, which is closely analyzed in section 3.3. Moreover, Fig. 3.19 illustrates the measured $s_v(\tau)$ as a function of VDL codes but with two-tone and five-tone inputs. f_{in} of 295 and 200-MHz are combined for two-tone input signal and f_{in} of 137, 177, 201, 214, and 251-MHz are combined for five-tone sinusoidal input signal. Even if the multi-tone input signal is employed, only a single minimum point exists and it proves that this technique can run in background with random wideband or narrowband signals. Moreover, both quadratic and linear relationship between $s_v(\tau)$ and τ are also found, depending on the magnitude of the timing skew. Fig. 3.20 and Fig. 3.21 illustrate the measured spectrum of the TI-ADC using two-tone and five-tone sinusoidal input signal before (left) and after (right) the calibration. After the calibration, all the timing-skew tones drop to below -63dBFS, which indicate that the timing-skew tones are eventually removed when the sample MAD reaches to the minimum.

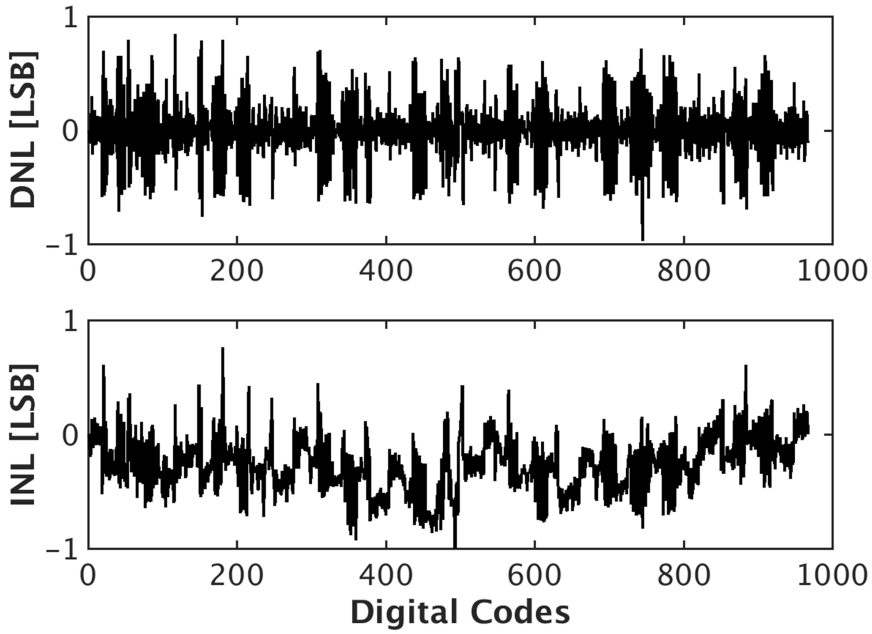

Figure 3.16: Measured DNL and INL of TI-ADC

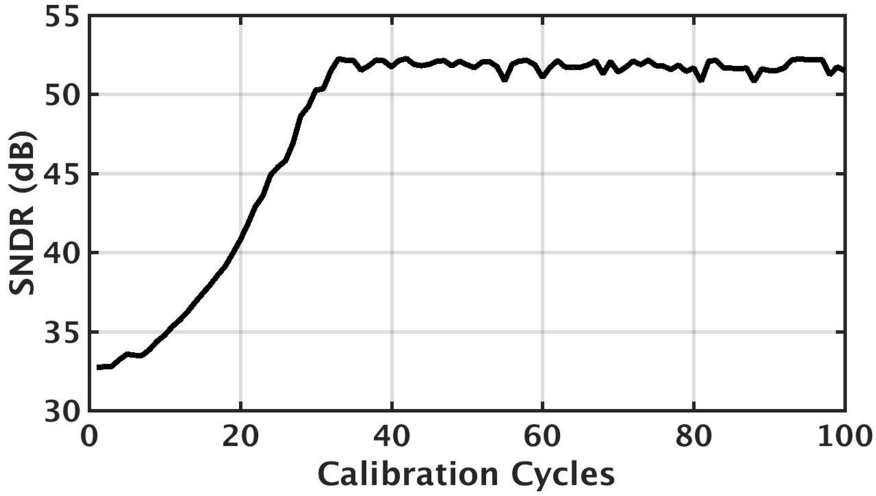

Figure 3.17: Measured SNDR versus calibration cycles.

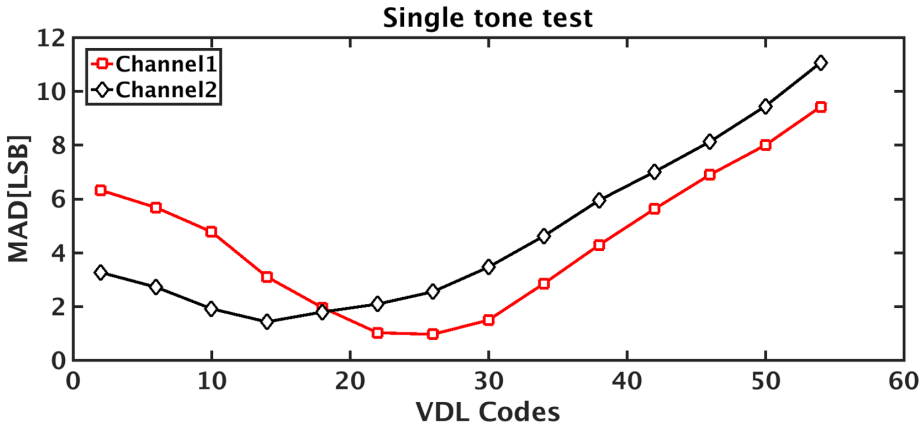

Figure 3.18: Measured MAD of inputs falling in the window versus VDL control code with a single-tone input.

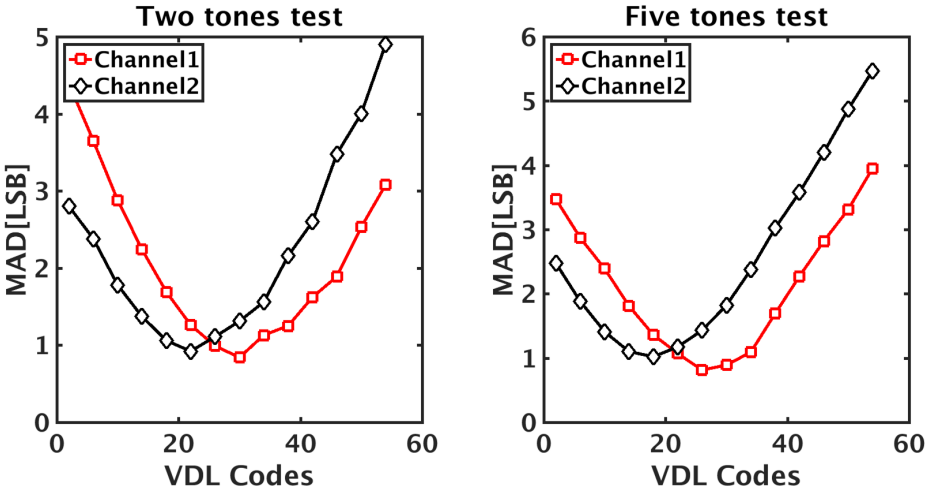

Figure 3.19: Measured MAD of inputs falling in the window versus VDL control code with a two-tone (left) and five-tone (right) inputs.

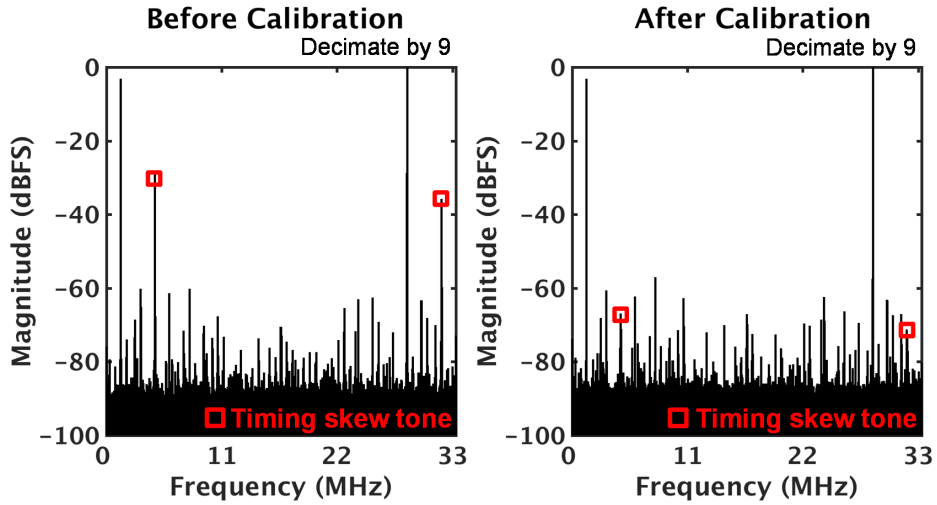

Figure 3.20: Measured spectrum of two tone input at 295MHz and 200MHz before and after timing-skew calibration.

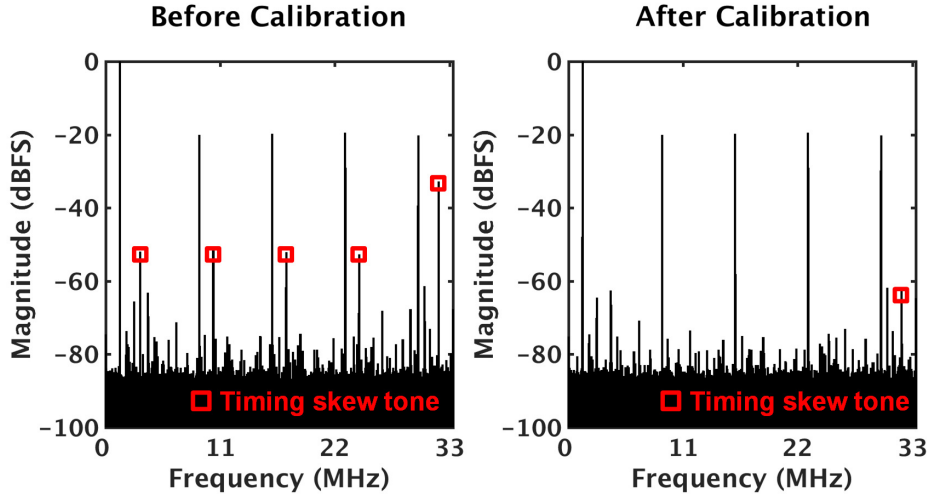

Figure 3.21: Measured spectrum of two tone input at 101, 137, 177, 201, 214, and 251MHz before and after timing-skew calibration.

Fig. 3.22 (left) shows the measured mean of $\{s_v(\tau)\}$ across 100 times measurements with a fullscale 295-MHz sinusoidal input. The measurement

results match well with $MAD(\tau)$ of (3.1). Fig. 3.22 (right) illustrates the fluctuation $\{\sigma_s(\tau)\}$ of 100 samples of $\{s_v(\tau)\}$. Moreover, Fig. 3.22 (right) shows the measurement results for $\sigma_s(\tau)$ with $M = 10^4$ and 10^5. The measurement results closely track $\sigma_s(\tau)$ derived in (3.5), which verifies the theoretical analyses of the proposed calibration technique. Measurement results used only about 200 output samples out of $M = 10^5$, which fall inside the window, for the computation of $s_v(\tau)$ of each channel. Thus, the amount of digital computation power is substantially lower than that of [22], which requires every ADC samples for the variance computation. Table 3.1 summarizes and compares the performance of the prototype ADC to previously published works. Overall, this work has achieved a Walden FoM of 23.8-fJ/conversion step at the Nyquist frequency and it is comparable to that of the state of the arts.

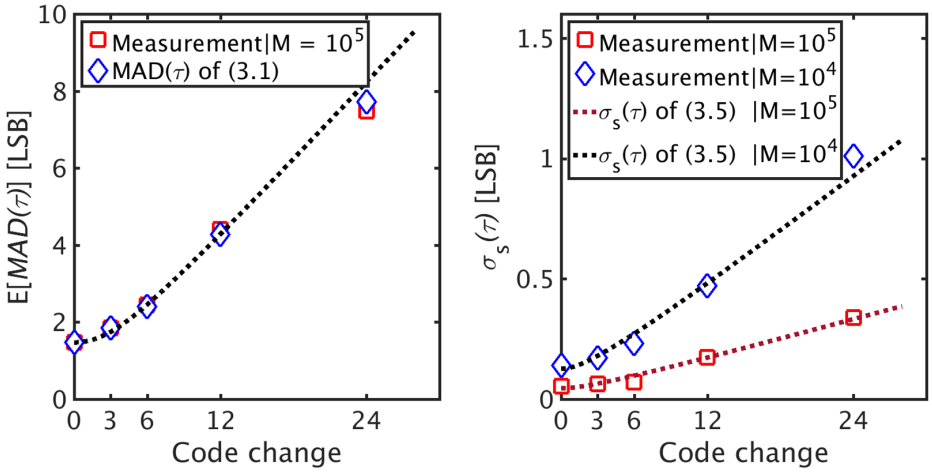

Figure 3.22: Measured mean $E[s_v(\tau)]$ (left) and fluctuation $\sigma_s(\tau)$ of 100 samples of $s_v(\tau)$ (right)

Parameters	**This work**	VLSI'10 El-Chammas	VLSI'12 Stepanovic	JSSC '14 Wei	ISSCC '14 Lee	ISSCC '14 Dortz	ISSCC '16 Lin
Architecture	**TI-SAR**	TI-FLASH	TI-SAR	TI-PIPELINE	FATI-SAR	TI-SAR	TI-SAR
Calibration technique	**MAD**	Cross correlation	Input slope estimation	**Auto** correlation	Variance	Input slope estimation	Auto correlation
Technology (nm)	**40**	65	65	65	65	40	40
Supply voltage (V)	**1.2**	1.1	1.2	1.2	1	1.1	1.1
Fs (GS/s)	**0.6**	12	2.8	4	1	1.62	2.6
# of sub channels	**2**	8	24	4	8	12	16
Sub channel fch (MS/s)	**300**	1500	117	1000	125	135	163
Resolution (bit)	**10**	5	11	8	10	9	10
Power (mW)	**4.7**	81	44.6	120	18.9	283	18.4
SNDR **@Nyquist (dB)**	**52.1**	25.1	50	44.4	51.4	48	50.6
FoM (fJ/conv-step)	**23.8**	460	78	219	62.3	283	25.6
Active area (mm^2)	**0.076**	0.44	0.63	1.35	0.78	0.83	0.825

Table 3.1: Performance summary and comparison.

Chapter 4

Conclusion

The thesis presents two different techniques that enhance the sampling rate of the SAR ADC: 2b/cycle conversion technique and time-interleaving technique. First chapter presented a 300MS/s single-channel 2b/cycle hybrid SAR with only 1 differential DAC. Unlike other previous works, this work shows the capability of 2b/cycle conversion with only 1 differential DAC array, which greatly reduces the hardware cost and area. The proposed SAR ADC takes advantage of 1b/cycle conversion mode and sufficient redundancy to address problems of multi-bit/cycle conversions, such as unmatched comparator offsets, kickback noise, and comparator input CM voltage variation. Reconfiguration to 1b/cycle is easily done by disabling the unneeded comparators for 1b/cycle conversion. This work achieves a peak Walden FoM of 19fJ/conv-step, which is in line with state-of-the-art SAR ADCs with single channel speed greater than 250MS/s. Second chapter presented a fast variance-based timing-skew calibration technique for TI ADCs. The proposed techniques use a simple low-power dynamic comparator and exploits the relationship between the comparator input and its decision time to identify ADC inputs that fall into a small window. By estimating timing-skew errors with only inputs falling inside the window, the estimation error is significantly re-

duced, leading to a substantially boosted convergence speed and substantially reduced the digital computation power. Moreover, because the comparator-based WD runs at full ADC rate, it does not periodically perturb the ADC input impedance. This chapter also presented the analyses of the signal and noise in the timing-skew calibration process and showed the advantage of having a small window width in accelerating the convergence. Both simulation and measurement results match well with those from analyses. The prototype 10-b 800-MS/s ADC in 40-nm CMOS achieves the Nyquist-rate SNDR of 48 dB and consumes 4.9 mW, leading to the Walden FoM of 29.8-fJ/conversion step. Last chapter presented a mean absolute deviation-based timing-skew calibration technique for TI ADCs. To maximize the convergence speed of the timing-skew calibration, a comparator-based window detector (WD) of [34] is utilized to suppress the timing-skew estimation errors and precisely estimate timing skews from orders of magnitude small number of samples than those of state-of-the-arts. In addition to all the advantages of the fast variance-based calibration technique, the proposed calibration technique eliminates the needs of squaring operations, which allows the removal of power-consuming multiplier and further reduces the digital computation power by almost 50% than that of variance-based calibration technique. After timing-skew calibration, a prototype 10-b 600-MS/s TI ADC in 40-nm CMOS achieves the peak SNDR of 56dB and 52 dB across the entire Nyquist band. Power consumption is 4.7mW and it leads to the Walden FoM of 23.8-fJ/conversion step.

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Vita

Jeonggoo Song was born in London, England. He attended American Community high School in Amman, Jordan. During his high school years, he served as a captain for the varsity badminton team and a student council secretary and president in his Junior and Senior year, respectively. He auditioned and got accepted as one of the two baritone-saxophone players in the International Music Festival held in Germany and Holland. After completing his work at American community School, Amman, Jordan, in 2006, he entered Rice University in Houston, Texas. In his freshman year, he played in Rice Owl marching band for one semester and he quit. He did not like it. After his junior year, he went back to South Korea to serve in the army for mandatory 2-year service. He came back to the US in 2010 and he received the Bachelor of Science degree in Electrical and Computer Engineering from Rice University. He joined the University of Texas at Austin as a graduate student in Fall 2012. Currently, he is working as a Component Design Engineer in Intel, Austin.

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